Abstract

Testing of high resolution second order sigma delta (??) modulator is a very expensive process. With the advanced technology, where the complexity over a small area is increasing, then testing at low cost with good accuracy is becoming a tedious issue for the manufacturing process. The cost effectiveness can be calculated on the basis of different parameters of the ?? modulator such as SNDR, ENOB, Gain, Offset, THD, SNR etc. Testing time also play an important role in the cost effectiveness of the modulator. The Built-in-self-test (BIST) allows the machine or circuit to test itself. BIST is desirable for the VLSI system in order to reduce the cost per chip of production –time testing by the manufacture, it can also provide the means to perform in-the field diagnostic. Therefore, this paper will demonstrate a possibility to simplify
modeling and simulation of testing strategy of high-resolution ?? modulator using MATLAB SIMULINK environment. Here, we are finding the cost effectiveness on the basis of Signal to Noise Distortion Ratio (SNDR) for the ?? modulator BIST. A ?? modulation based signal generator is considered which can produce analog sinusoidal test stimuli and digital reference signal on chip. By comparing the ADC output with that of the generator reference signal, the parameter can be determined on chip based on the standard equations in the proposed simulation environment.

References

- Shaoyu U. K, Yan Han, You Cai A 3.3V 18 Bit Digital Audio Sigma-Delta ADC in 0.18um CMOS Process 2007
Index Terms

Computer Science  Circuits And System

Keywords
Sigma Delta Modulator  Built-in-self-test  Sigma Delta Adc