Abstract

During synthesis of power gated finite state machine (FSM) power can be reduced by reducing switching activity of the implemented circuit. Power gating can be applied to turn OFF the inactive sub-machine which is obtained after partitioning the FSM by gating the supply voltage. During transition from the states of one sub-machine to other sub-machine, wakeup time is required to turn OFF the current sub-machine and turn ON other. Wakeup time affects the partitioning of FSMs for its power gated implementation as both the sub-machines are ON during this time. In this paper, we have calculated this wakeup time to find the boundary depth. Variation of wakeup time as a function of size of sleep transistor and sub-machine has also
been studied. Power model has been developed for the power-gated design of FSM. Here, we present a Genetic Algorithm (GA) based solution of the problem of both partitioning and encoding of power gated FSM for reduced power consumption. Experimental results show that more than 55% power can be saved in this approach.

References


Index Terms

Computer Science VLSI Design

Keywords

Finite State Machine Partitioning Power Gating Wakeup Time Boundary Depth Power Model
Low Power