Abstract

System on Chip (SOC) designs offer integrated solutions to existing design tribulations in areas which necessitate outsized computation and restriction in certain area. But the performance of these has been sluggish due to the restriction of the common bus architecture espoused by these systems and thereby low processing speeds. This has been the main drawback for scalability in terms of computation and enhancement in
Implementation of An Effective Router Architecture for NoC on FPGA

its performance. With the advancement in semiconductor devices and fabrication technology, it is possible to pack more logic in smaller area of silicon. But the implementation of these mega functional modules using common bus architecture, parallel bus architecture, pipelining are becoming ineffective and posing a bottleneck in terms of performance and throughput in this billion transistor era. As a solution for this problem, Network on chip is being adopted in this paper as the core bus architecture across different spectrum of SOCs.

This work presents a simple design using FPGA based system. Hence, it is a very flexible network design that will accommodate to various needs. This router is implemented for four topologies and compared for its speed area and power consumption.

Reference


Index Terms

Computer Science Wireless Networks

Key words

- on-chip topology
- Packetization
- Router Architecture