Abstract

The full adder circuit is the major cell in many processing Systems. The full adder is used to add the partial products of multipliers. Decreasing the number of transistor count in full adder can result in the less power consumption. In this paper different types of full adders has been implemented by using cadence virtuoso 180nm and 90nm technology this results decreasing the total power consumption of full adder.
Comparative Analysis of Different Types of Full Adders using 180nm and 90nm Technology

References


Index Terms

Computer Science

Circuit And Systems

Keywords

Full Adder     Adiabatic Logic     28t     20t     14t     Half Adder