Abstract

A SAR ADC is presented in this paper with low power consumption. In this paper an asynchronous SAR logic is used which will reduce its power consumption as MSB bit evaluation and each bit evaluation time is different, due to which it provide high resolution for same power consumption. A dynamic comparator is used. It doesn't consume any static power which will reduce its power consumption. Vcm-based switching technique reduces its power as it maintains the common mode voltage. In this paper different block of a SAR ADC with their schematics and wave-forms is presented. This work is done by using Synopsys Galaxy Custom Designer Tool using 90nm CMOS technology in which power consumption by DAC is 33uW, Comparator consumes 43uW, SAR Logic consumes 55uW with frequency range 100MHz.
References

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Index Terms

Computer Science
Circuit System

Keywords
Sar  Lower And Upper Dac  Sample And Hold Circuit  Bootstrapped Switch