Abstract

In Network-on-chip router is the main block where one of the major decisions about the route direction is taken. This paper presents asynchronous router implemented using handshaking signals. Distributed routing with 3X3 Mesh topology is used in this design. 2D Mesh is the most common topologies due to its grid-type shape and regular structure which is most appropriate for the two dimensional layout on a chip. The design is synthesized for the Stratix II EP2S15F484C3 FPGA using Quartus II software. The router supports maximum of five simultaneous routing requests.
Asynchronous Router for Network-on-Chip on FPGA

References


Index Terms

Computer Science

Networks

Keywords

Network On Chip; Wormhole Switching; Xy Routing Algorithm; Asynchronous Router