Abstract

The Network-on-Chip is a packet switched platform for single chip systems which scales well to an arbitrary number of processor like resources. The network-on-chip (NoC) design paradigm is seen as a way of enabling the integration of an exceedingly high number of computational and storage blocks in a single chip. This provides vertical integration of physical and
architectural levels in system design. A chip consists of contiguous areas called regions, which are physically isolated from each other but have special mechanism for communication among each other. The NOC architecture essentially is the on-chip communication infrastructure comprising the physical layer, the data link layer and the network layer of the OSI protocol stack. NOC architecture, a general purpose on-chip interconnection network replaces the traditional design- specific global on-chip wiring, by the use of switching fabric or routers to connect IP cores or processing elements (PEs).

Reference


Index Terms

Computer Science  Image Processing

Key words

Packet switching  On

chip communication  NOC design

NOC