Abstract

Efficient algorithms and architectures are existing for the design of low-complexity bit-parallel multiple constant multiplication (MCM). This operation dominates the complexity of many digital signals processing system. Alternative to this, digit-serial MCM design is available with less complexity. But it is not as much popular as the former one. In this paper, the gate –level area and power of digit-serial MCM design is tried to optimize. So initially from the basic parallel
Enhancing Driving Direction Time based on speed fluctuation and Vehicle Type Identification

designs, like shift –adds implementation, the common sub-expression elimination and graph-based method are used. From this the efficient one is selected, that is the GB technique and is applied to digit-serial design. Then the newly designed MCM block will be placed to the multiplier block of an FIR filter. Thus comparing to bit-parallel FIR filter design, digit-serial design has 41% of power reduction and 40.5% of area reduction and are independent of data word-length.

References

Enhancing Driving Direction Time based on speed fluctuation and Vehicle Type Identification


Index Terms

Computer Science

Data Mining

Keywords

Digit-serial Arithmetic Finite Impulse Response (fir) Filters Multiple Constant Multiplications (mcm).