Certain Investigations on Power Performance in Nanoscale CMOS Digital Circuits with Low Leakage Design Techniques

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Authors:

Greeshma. V

R. Udaiya Kumar

Abstract

In this paper, it is attempted to analyze the power performances of few CMOS digital circuits such as full adder, multiplexer and SRAM cell with the inclusion and redesign of ultra low leakage (ULL) techniques. The basic principle behind this ULL is based on a pair of source-connected N-MOS and P-MOS transistors, automatically biasing the stand-by gate-to source voltage of N-MOSFET at negative and P-MOSFET at a positive voltage levels, thereby pushing the leakage current towards its physical limits. Virtual ground concept is also introduced to reduce the power dissipation further. The circuits are designed with DSCH schematic design tool using CMOS 90nm technology and simulations are performed by using...
Level3 model files. The final layout of all circuits is generated using microwind. From the obtained results, a significant amount of power reduction is noticed without other functional performances such as area and speed are getting affected.

References

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Index Terms

Computer Science  Networks
Keywords
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