Abstract

Field programmable gate arrays are ideally suited for the implementation of DCT based digital image compression. However, there are several issues that need to be solved. The Multiply-Accumulate Unit (MAC) is the main computational kernel in DSP and DIP architectures. The proposed MAC unit determines the power and the speed of the overall system; it always lies in the critical path. In this work, a fast and low power MAC Unit is proposed for 2D-DCT computation. The proposed architecture is based on modified booth radix-8 with merged MAC architectures to design a unit with a low critical path delay. The new architecture has reduces the hardware complexity of the summation network, it reduce the overall power. Increasing the
High Speed Radix-8 based MAC for 2D-Image Compression

speed of operation is achieved by feeding the bits of the accumulated operand into the summation tree before the final adder instead of going through the entire summation network. The FPGA implementation of the proposed booth radix-8 based MAC unit saves 64% of the area, to the regular MAC unit with conventional multiplier.

References

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Index Terms

Computer Science

Image Processing

Keywords

Discrete Cosine Transform (dct) Very Large Scale Integration (vlsi) Digital Signal
Processing (dsp)
Multiply-accumulate Unit (mac).