Abstract

Floating-point operations are of great use for many computing applications involving large
dynamic range, but importantly it needs more resources as compared to integer operations.
The progressive demand in FPGA innovation makes such gadgets progressively alluring for
designing FP units. With the expanding limitations on delay, more attention is being given to
configuration of quicker FP units. To improve speed a wide range of mechanisms/methods are
being utilized for the designing of FPU (Floating point math unit) with the aim of reducing
latency, area, power consumption and increasing the throughput. Some of the algorithms are
presented in this paper, which enlightens the above-mentioned aim.
References

- Stuart Franklin Oberman, DESIGN ISSUES IN HIGH PERFORMANCE FLOATING POINT ARITHMETIC UNITS, Technical Report, Stanford University California, 1996.

Index Terms
Keywords
Floating Point Adder  Floating Point Subtraction  Floating Point Multiplier  Floating Point Square  Vedic Sutras