Abstract

Testing of combinational circuit is crucial important to ensure high level of functionality. As density of digital circuit increases rapidly day by day these increases cost and time to test a particular combinational circuit for testing such circuit we need high quality test vector pattern with minimum number of input combination. In this work, we are designing Automatic test pattern generator (ATPG) D_Algorithm which will generate a minimum number of input pattern to detect fault like stuck-at-0 fault, stuck-at-1 fault, short circuit fault. D_Algorithm has been design by writing practical extraction and report language script to generate VHDL coding which is simulated on Xilinx 9.1.
References

- Joe Dunbar "FPGA Based Design for Accelerated Fault-Testing of Integrated Circuits." &quot;Bucknell University Jan 2010

Index Terms

Computer Science

Algorithms
Keywords

Atpg (automatic Test Pattern Generator)  Fpga (field Programming Gate Arrays)  Fate (fpga Based Automatic Test Equipment)

Cut (circuit Under Test)