Abstract

Flip-flops and latches are the most important elements of a design for both a delay and energy point of view. In many electronics design low power consumption is basic need in most of the applications. The energy performance requirements enhance the most designers of next generation system towards the least possible power consumption. The power consumption is basically reduced by scaling of a power supply voltage. Flip flops typically consumes more than 50% of random logic power in the SoC chip, because of redundant transition of internal node. A
low power flip flop design featuring pulse triggered structure based on signal feed-through scheme is presented which successfully solves the long discharging path problem in a various pulse triggered flip flop design and achieve a better power performance and better speed. In this paper we have studied all the major techniques to achieve a low power flip flop and presented their comparison.

References

- S. Sadrossadat, H. Mostafa, and M. Anis, Statistical design framework of sub-micron

**Index Terms**

Computer Science                  Signal Processing

**Keywords**

Flip-flops  Low Power  Pulse Triggered  Leakage Power  Pipelining.