Abstract

Adders are the basic unit of arithmetic operations. Due to the rapidly growing mobile industry not only the faster arithmetic unit but also reduced area and low power arithmetic units are needed. The CMOS carry select adder (CSLA) consists of two sets of ripple carry adder (RCA) and the modified CSLA replaces one set of RCA with a binary to Excess One (BEC) converter. The modified carry select adder architecture has developed using Binary to Excess-1 converter
Design and Verification of Carry Select Adder in 180nm CMOS Technology

In this paper design of 16 bit modified carry select adder has been designed.

References

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Index Terms

Computer Science  Signal Processing

Keywords

Area Efficient  CSLA  Low Power And  BEC