Abstract

Wallace Tree Multiplier (WTM) is the fastest multiplier used in number of data-processing processors to perform fastest arithmetic function. From the structure of the RCWM Reduced Complexity Wallace Tree Multiplier, it is clear that there is scope of reducing the power consumption and area. This work uses an efficient and simple gate-level modification to significantly reduce the power and area of RWTM. Conventional WTM is still area-consuming
due to the CMOS switching structure. The logic operations involved in conventional RCWM and WTM are analyzed to study the data dependence and to identify redundant logic operations. RCWM reduced number of half adders used in Standard Wallace Multiplier (SWM) with slight increases in full adders to reduce the multiple numbers of gates. Adiabatic Logic eliminated all the redundant logic operations present in conventional RCWM. Experimental analysis shows that this architecture achieves the three folded advantages in terms of power and area.

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Keywords
Adiabatic Logic  Wallace Tree Multiplier  Tanner Tool  16×16 Multiplier.