Abstract

Caching is a fundamental technique commonly employed to hide the latency gap between
memory and the CPU by exploiting locality in memory accesses. On today’s architectures a cache miss may cost several hundred CPU cycles [1]. In a two-level memory hierarchy, a cache performs faster than auxiliary storage, but is more expensive. Cost concerns thus usually limit cache size to a fraction of the auxiliary memory’s size. This paper represents a comparative predictability about some of the traditional and new replacement techniques in contrast with OPTIMAL replacement technique.

References

- Figure 2: Performance Analysis of different techniques using Average Hit Ratio.
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Analysis and Predictability of Page Replacement Techniques towards Optimized Performance

- Development of a Virtual Memory Simulator to Analyze the Goodness of Page Replacement Algorithms Fadi N. , Sibai, Maria Ma, David A. Lill
- The LRU-K Page Replacement Algorithm For Database Disk Buffering Elizabeth J. O'Neil 1, Patrick E. O'Neill, Gerhard Weikum2 SIGMOD 15193 AVaahin~ton, DC,USA @1993ACM.

Index Terms

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Keywords
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