Low Power Conditional-Capture Flip-Flop with Clock Gating

Abstract

A low power clock gated conditional capture flip-flop is proposed. Conditional capture flip-flop has redundant transitions due to continues flow of clock signal irrespective of logic levels of the input and the output and also consumes more power [1, 2]. In order to reduce the redundant transitions in the conditional capture flip-flop clock gating concept is used [3]. A clock gated conditional capture flip-flop consumes less power than the conditional capture flip-flop. The
proposed flip-flop achieves power savings of up to 75% with better performance. The proposed flip-flop also has more negative setup time than the conditional capture flip-flop and provides less propagation delay. The power analysis of the circuit is simulated using HSPICE in 0.18 um technology.

Reference


Index Terms

Computer Science Wireless

Key words

Low Power Conditional-Capture Flip-Flop
Clock Gating