Abstract

This paper presents two new 1-bit full adder cells operating in subthreshold region with 65nm, 90nm and 0.18um technologies. Circuits designed in this region usually consume less power. Inverse Majority Gate (IMG) together with NAND/NOR were used as the main computational building blocks. A modification was done to optimize W/L ratios with different supply voltages. We used W/L ratios for all the PMOS transistors 1.5 times the ratio of W/L for all NMOS
transistors. Compared with a previously reported minority-3 based full adder; the results involve better performance in terms of power, delay, and PDP.

Reference

- Razavi, B. Design of Analog CMOS Integrated Circuits.

Index Terms

Computer Science Wireless
Design of Two Full Adder Cells in Subthreshold Region by Various CMOS Technologies and Compare Together

Key words

VLSI

Subthreshold
full adder

inverse majority gate