Abstract

Due to rapid advances in VLSI design technology during the last decade, the complexity and size of circuits have been rapidly increasing, placing a demand on industry for faster and more efficient CAD tools. Physical design is a process of converting the physical description into geometric description. Physical design process is subdivided into four problems: 1. Partitioning, 2. Floor planning 3. Placement and 4. Routing. Placement phase determines the positions of the
cells. Placement constrains are wire-length, area of the die, power minimization and delay. For the area and wire length optimization a modern placer need to handle the large-scale design with millions of object. This thesis work aims to develop an efficient and low time complexity algorithms for placement. This can be achieved by the use of a problem specific genotype encoding, and hybrid, knowledge based techniques, which support the algorithm during the creation of the initial individuals and the optimization process. In this paper a novel hybrid genetic algorithm, which is used to solve standard cell placement problem is presented. These techniques are applied to the multithread of the VLSI cell placement problem where the objectives are to reduce power dissipation and wire length while improving performance (delay).

Reference

An Analogous Computation on Hybrid Genetic Algorithm for VLSI Physical design Specific to Placement Problem


Index Terms

Computer Science Wireless

Key words

VLSI design physical

design placement

standard cell

multithread