Abstract

In this paper, two high performance full adder circuits are proposed. We simulated these two full adder circuits using Cadence VIRTUOSO environment in 0.18 μm UMC CMOS technology and compared the Power dissipation, time delay, and power delay product (PDP) of the proposed circuits with other 10 transistor full adders. Simulation results show that for the supply voltage of 1.8V, these circuits are suitable for arithmetic circuits and other VLSI applications.
On the Design of High-Performance CMOS 1-Bit Full Adder Circuits

with very low power consumption and very high speed performance.

Reference


Index Terms

Computer Science Wireless
Key words

CMOS logic

Full

adder

High-performance

Threshold loss