Abstract
Adders are representative of signal processing architectures. In this paper three low power Asynchronous Full Adder circuits are proposed. Asynchronous circuits make it suitable for low power operation of the circuits. Asynchronous circuits stops computing when there is no change in the input there by eliminating the need for extra complexity of clock gating. Low power and low energy techniques such as minimizing the number of transistors, voltage scaling are used. The implication of voltage scaling is a wide range of variation in the delay. The reduction in power also minimizes the efforts for the heat dissipation and cooling expenses. The reduction in power also minimizes the efforts for the heat dissipation and cooling expenses. Asynchronous Adder circuits dissipate less power in applications where performance is non-limiting. Asynchronous adders can be implemented using static or dynamic circuits. Asynchronous dynamic adder circuits employ a single rail or dual rail logic or a combined logic. The Circuits are implemented using cadence 90nm Technology and simulated using Spectre simulator. The delay achieved is 36ps, 39.6ps, 35.9ps as compared to 239ps for PTL Adder when 1.2v supply voltage is considered the average power dissipated is 146nw, 153.6nw, 150.9nw and the power delay product (PDP) obtained is 5.25e-18, 6.09e-18, 5.43e-18 as compared to PTL adder which is 46.8uw and 5.4e-15. There is a considerable amount of reduction in the Average Power dissipated, Delay and PDP for all the three proposed adders compared to PTL Adder when the supply voltages of 1.5v, 1v, and 0.7v are used.

Reference


Index Terms

Computer Science

Wireless
High Speed Power Efficient Asynchronous Adders

Key words

Asynchronous
low power
delay

Full Adder

Pass Transistor
Dynamic
static
XOR gate