Abstract
The complexity of the circuits design is growing rapidly with the increasing demand of electronics products in the market. The time available to design a product is shrinking because of competitive pressures. Considerable amount of money get spend in developing an electronics design. FPGA environment is the best solution to address all such issues. In this work FPGA, Matlab, and ISE 9.1i such low cost tools are used to design 14 bit, 20 MSamples/s, 85 mW successive approximation analog-to-digital converter (ADC) suitable for RF applications. Matlab’s Simulink is used to generate VeriLog code for ADC. The design is simulated and synthesized using Xilinx’s ISE 9.1i and finally results are tested on Xilinx’s Spartan II FPGA.

Reference

- Data sheet AD7940 from Analog Devices.
- Data sheet LTC1411 from Linear Technology.

Index Terms

Computer Science Wireless
Key words

ADC
ISE9.1i
Simulink
System generator

FPGA