Abstract

The paper presents a novel method of structure for designing and implementation of hardware reduced FIR filter in mixed signal processing domain for parallel data processing. Supported by a review of the literature, the paper demonstrates that the proposed methodology is superior, economical and can be applied in to applications like bio-medical and audio signals. The results show improved performance and cost reduction, which has practical implications in terms of applications.
References

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Index Terms

Computer Science

Emerging Trends in Technology
Keywords
Mixed Domain  Hardware FIR  Multipliers  adders  integrator  summing  integrator  scaling  resistors

decimation algorithm
stopband
and sinusoidal wave.