Abstract

This paper presents 1-bit CMOS full adder cell using standard static CMOS logic style. The comparison is taken out using several parameters like number of transistors, delay, power dissipation and power delay product (PDP). The circuits are designed at transistor level using 180 nm and 90nm CMOS technology. Various full adders are presented in this paper like Conventional CMOS (C-CMOS), Complementary pass transistor logic FA (CPL), Double pass transistor logic FA , Transmission gate FA (TGA), Transmission function FA, New 14T,10T, Hybrid CMOS, HPSC, 24T, LPFA (CPL), LPHS, Hybrid Full Adders.
Full Adder Circuits using Static CMOS Logic Style: A Review

References

- Ming-Bo Lin, "Introduction to VLSI systems A logic, circuit and system perspective," Taylor & Francis group, ch. 7.
Full Adder Circuits using Static CMOS Logic Style: A Review


Index Terms

Computer Science

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Keywords

Pdp  CMOS Full Adder  Power Dissipation  Low Power  Delay