Abstract

SRAM is the most crucial part of memory designs and are imperative in many simple or compound applications that implicate system on chip (SoCs). Power dissipation and stability has now become the most essential area of concern in sub-micron SRAM cell design with continuous technology scaling according to Moore’s law. At latest, retrenchment of channel length MOSFET is directly proportional to the new technologies generating step by step with new innovative tools. With an improvement in technology there is a sudden retrenchment of channel length of MOSFET. Moreover, in this network of stability SRAM has become very essential and major area to research in. Static noise margin generate its crucial role in the
stability of SRAM. This paper introduce to the basic 6T SRAM cell. The outperforms of this SRAM cell in elaboration with transient response and static noise margin is described with the counter fit results using the EDA tool Custom Designer at 90nm CMOS Technology.

References


Index Terms

Computer Science, Circuit And Systems
Keywords
- Static Random Access Memory (sram)
- Cmos
- Static Noise Margin (snm)
- Read Noise Margin
- Write Noise Margin
- Wordline
- Bitline.