Abstract

Low power device design has become a significant field of research due to increase used of portable devices. In this paper, various D flip-flop topologies have been scrutinized for
estimation of propagation delay (tp) and power dissipation (Pdis) and delay variability for portable applications. High level triggered D flip-flops have been considered for analysis. Today's electronic devices require high speed design feature with minimum power dissipation. Design for variability has become vital as relative level of parameter and device variability has been increasing with device density scaling. In this paper, delay variability of the flip-flops has been investigated at 16-nanometer CMOS process on SPICE.

References

Keywords
Delay Variability  Energy-delay Tradeoff  Flip-flops  Differential Logic Families