Abstract

This paper presents design and implementation of a Pipelined FFT Architecture using Verilog HDL. The Pipelined Architecture is implemented using RS2DF (Radix-2 Single path Delay Feedback). Standard FPGA Flow is adapted to implement and was programmed on Spartan 3AN FPGA. Simulations and Synthesis are carried using Modelsim and Xilinx ISE. The Verilog Simulations results are compared with Inbuilt MATLAB FFT Core for verification of the design. The Speed achieved for this Core is 87.15 MHz.

References
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**Index Terms**

Computer Science

Algorithm

**Keywords**

Fft    Spartan 3    scalable Architectures    fpga    dft