Abstract

This paper presents design and implementation of a Pipelined FFT Architecture using Verilog HDL. The Pipelined Architecture is implemented using RS2DF (Radix-2 Single path Delay Feedback). Standard FPGA Flow is adapted to implement and was programmed on Spartan 3AN FPGA. Simulations and Synthesis are carried using Modelsim and Xilinx ISE. The Verilog Simulations results are compared with Inbuilt MATLAB FFT Core for verification of the design. The Speed achieved for this Core is 87.15 MHz.
- ShouSheng and MatSTorKelson. A New Approach to Pipeline FFT Processor, IEEE proceedings of IPPS 1996.
- ZE KeWaA, XuE Liu, FeNg YU. Pipelined Architecture for Normal Input /Output Order FFT, JZUS, C-2011.
- DavldHwAng, YinGningPeNg, Pipeline FFT Architectures Optimized For FPGA, International Journal, Volume 2009 (2009),
- VeNuGoPal B, VasAnthaSudHeer N, FPGA Implementation Of 64 Point FFT Processor, IJIT and Exploring Engineering ISSN: 2278-3075, SEPTEMBER 2012.

**Index Terms**

Computer Science

Algorithm

**Keywords**

Fft  Spartan 3  scalable Architectures  fpga  dft