Abstract

Finite impulse response (FIR) filters are tremendously used in signal processing applications like RADAR processing, noise cancellation, biomedical imaging, removing DC component in signal etc. Most of Digital signal processing algorithm such as FFT,FIR and IIR are now implemented on FPGA because it offers very attractive solutions than any other in terms area, power and speed. Reconfigurable architecture used in this paper is Distributed arithmetic. Here DA based FIR filter implemented on vertex5 with device XC5VLX110T. DA based FIR filter proposes advancement in speed, performance and area.
- Sang Yoon Park, Member, IEEE and Pramod Kumar Meher, Senior Member, IEEE "Efficient FPGA and ASIC realization of DA based reconfigurable FIR digital filter" IEEE transaction on circuit.
- Yajun Zhou, Pingzheng Shi School of Automation, HangZhou Dianzi University "distributed arithmetic for FIR filter implementation on FPGA. 978-1-61284-774-0/11/$26IEEE.
- Saliha Harize, Mohamed Benouaret, Noureddine Doghmane "A methodology for implementing decimator FIR filters on FPGA" ELSEVIER publication.
- J. L. Mazher Iqbal. And S. Varadarajan "New approach to memory less design and look up table realization for low complexity reconfigurable Digital filter architecture" WSEAS transactions on system.

**Index Terms**

Computer Science  
Algorithm

**Keywords**

Da-distributed Arithmetic  
Fpga-field Programmable Gate Array  
Radar –radio Direction And Ranging.