Abstract

The sensor network has become an important aspect in the day today life because of its wide range of application from medical field to the military application. The raw data from sensor node are of large quantity and hence it is necessary to store these data bits. In this paper, design of optimized SRAM array for low power applications is implemented. SRAM cell is designed using 8T. In this, transmission gate is used as access transistor to increase write-ability and decrease the power dissipation. The peripheral circuits are chosen to construct the SRAM array. Simulation are carried out using 180nm technology and result show that the reading and writing of data takes place correctly.

References

- Vazir, Irina, et al, "SRAM IP for DSP/SoC Projects" Diss. San Jose State University SRAM.
- Chang et al. "A differential data-aware power-supplied (D2AP) 8T SRAM cell with expanded write/read stabilities for lower VDD min applications" vol 45, 1234--1245, IEEE 2010.
- M. Yabuuchi et al. "A 45 nm 0. 6 V Cross-Point 8T SRAM with Negative Biased Read/Write Assist" Symposium on VLSI Circuits Digest of Technical Papers, IEEE 2009, pp. 158--159.

Index Terms

Computer Science
Power Systems

Keywords
Sram  Sensor Network  Static Noise Margin.