Abstract

The transmission of the data with traffic free, low latency and high throughput from source to destination are the challenges for on chip multi processing system on chip (MPNOC) design. The conventional packet switching approach having large amount of power and area for the queuing buffer. Topologies such as mesh and torus[10], are intuitively feasible for physical layout in a 2-D chip. Having the high wiring irregularity and the large router radix of indirect topologies such as Benes or Butterfly[11], pose a challenge for physical implementation. The present work, the silicon-proven design of a novel on-chip network to support guaranteed traffic permutation in multiprocessor system on chip applications. The proposed network employs a pipelined Circuit switching approach combined with a dynamic path setup scheme under a multistage network topology. The dynamic path-setup scheme enables runtime path arrangement for arbitrary traffic permutations. The circuit switching approach offers a guarantee of permuted data and its compact overhead enables the benefit of stacking multiple networks. Design and developed by using XILINX 12.4 and simulated on Modelsim 6.3f and implemented on Spartan 3 FPGA Device. This can achieve high throughput, low latency and low cost.

References

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Index Terms

Computer Science

Networks

Keywords

Permutation Network  Circuit Switching  Dynamic Path Setup Scheme  And System On Chip And Network Topology.