Abstract

In VLSI, scaling methods plays an important role in reducing the power dissipation from one technology node to other technology node. The two major constraints for delay in any VLSI circuits are latency and throughput. The negative bias temperature instability (NBTI) effect occurs when a pMOS transistor is under negative bias (Vgs= -VDD) increasing the threshold voltage of pMOS transistor and reducing the speed. A similar phenomenon, positive bias temperature instability (PBTI) effect occurs when an nMOS transistor is under positive bias. These both effects degrade the transistor speed and system may fail due to timing violations. In this paper, an Adaptive Hold Logic (AHL) circuit is proposed to mitigate the performance
Design of Adaptive Hold Logic (AHL) Circuit to Reduce Aging Effects

degradation due to aging effects.

References


- S. Khan, H. Kukner, P. Raghavan and F. Catthoor, "BTI Impact on Logical Gates in Nano-scale CMOS Technology".

Index Terms

Computer Science Circuits And System
Keywords
Aging Effects  Aging Indicator  Bias Temperature Instability.