Abstract

The requirements of low power integrated circuits are very important in all electronic portable equipment’s. Normally SRAM consume more power during read and write operations because of more power consumptions speed of the circuit will be reduced finally the performance will be degraded. To reduce power consumption and increase RNM (Read Noise Margin) the adiabatic change of word line voltage is used in single bit line SRAM and also sense amplifier flip flop and pre-charge circuit is used. During read operation pre-charge circuit is connected with selective bit lines to minimize the overall RAM power consumption and sense amplifier flip-flop is used to increase the speed of the operation. Using of adiabatic circuit in
single bit line SRAM, the power consumption is reduced from 80% to 50%.

References

Design of Low Power Sram using Adiabatic Change of Wordline Voltage


**Index Terms**

Computer Science

Circuits And System

**Keywords**

Sram  Rnm  Sense Amplifier Flip Flop  Adiabatic Logic.