Abstract

Scaling of conventional CMOS devices has reduced the device dimensions from 10 mm in 1970s to 0.1 \( \mu \)m in a present day. According to ITRS (i.e. International Technology Roadmap for Semiconductors) we are going to face the brick wall in 2015 if we continue in the same development speed. This will not be possible for us to maintain the pace forecasted by Moore's law. This is because of the fundamental limitations of device parameter...
dimensions due to which performance is degrading in several ways. To overcome this and go ahead in technology, one must look into new devices those can be scaled down to come up with other solutions. Either it should be possible to go ahead by again reducing the device dimensions in some way or we have to reduce the circuit overhead with less complexity. Solution to this might be: MVL i.e. Multi-valued Logic & TFET i.e. Tunnel Field Effect Transistor.[1] This report presents a novel design of Ternary Logic Gates & arithmetic circuits using TFET.

References

- Low power CMOS circuit design: by Kaushik Roy
- CNTFET based design of Ternary Logic Gates & Arithmetic Circuits: by Sheng Lin, Student Member, IEEE; Yong-Bin Kim, Senior Member, IEEE, and Fabrizio Lombardi, Fellow, IEEE.
- Aspects of balance Ternary Arithmetics implemented using CMOS charged semiconducting Gate Devices: by Henning Gundersen, Institute of informatics, University of Oslo.
- A Novel CNTFET-Based Ternary Logic Gate Design: by Sheng Lin, Yong-Bin Kim and Fabrizio Lombardi, Northeastern University Boston, MA, USA.

Index Terms

Computer Science

Engineering and Technology

Keywords

CMOS ITRS TFET MVL