Abstract

In this paper, we present Energy efficient CMOS full adder, which is one of the basic building blocks of a modern electronic systems design. Energy-Efficiency is one of the most required features in digital electronic systems for high-performance and/or portable applications which signify PDP, it measures the energy consumed per switching event. This paper shows that complementary CMOS is the logic style of choice for the implementation of combinational
circuits, if low voltage, low power, and small power-delay products are of concern with relatively low area.

References


Index Terms

Computer Science

Network Application
Keywords
Adders  Cmos Full Adder  Low Power  Vlsi  High-speed  Low-area.