Abstract

Low power design has become the major challenge of present chip designs as leakage power has been rising with scaling of technologies. As the demand for low power and low cost increases, it is very important to design low power, high performance, and fast responding SRAM (Static Random Access Memory) since they are critical component in high performance processors. The Conventional 6T SRAM cell is very much prone to noise during read operation[2]. To overcome the problems in 6T SRAM cell, researchers have proposed different SRAM topologies such as 8T, 9T, 10T etc. bit cell design. These designs can improve the cell stability but suffer from bit line leakage noise. Dynamic power was previously the single largest concern for low-power chip designers, but as the feature size shrinks, the leakage power
Design and Power Analysis of Memory System using Conventional 6T, Sleepy Stack 8T and Single Ended 6T SRAM cell

reduction has become the great challenge for current and future technologies. In this paper, different SRAM cells are used for the power analysis and also single ended 6T SRAM is introduced which reduces the power and area considerably.

References

- Nahid Rahman, B. P. Singh "Design of low power SRAM Memory Using 8T SRAM Cell" - IJRTE.
- Bhavya Daya, Shu Jiang, Piotr Nowak, Jaffer Sharief "Synchronous SRAM Design", Electrical Engineering Department, University Of Florida.

Index Terms

Computer Science

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Keywords

Sram Cell   Pre-charge Circuit   Sense Amplifier   Single Ended Sram Cell

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