Abstract

The Adder is the important part in any processor/controller design. Till date there are a plenty of 1-bit full-adder circuits which have been proposed and designed. In this paper we have a
analytic and comparative description of various full adder circuits, considering various constraints like power consumption, speed of operation and area. The circuits are designed in the virtuoso platform, using cadence tool with the available GPDK – 45nm kit. The Full-adder circuits with the most 28 transistor to the one with only 6 transistors are successfully designed, simulated and compared for various parameters like power consumption, speed of operation(delay) and area (transistor count), and finally concluded the best designs, that suite for the particular specifications.

References


**Index Terms**

Computer Science  
Circuits And Systems

**Keywords**

Cadence  
Virtuoso  
Gpdk  
Delay  
Power Consumption  
Area (transistor Count)