Abstract

In this work, a CODEC design to eliminate/reduce the propagation delay across long on chip buses which are increasingly becoming a limiting factor in high-speed design has been proposed. Crosstalk between adjacent wires are transitioning in opposite direction create a significant portion of this delay. The coding scheme is based on the Fibonacci numeral system. The proposed CODEC design is efficient and a modular technique. Encoding and decoding algorithms are proposed for three different Fibonacci techniques. The experimental results show that the proposed CODEC reduces crosstalk delay when compared to that of existing approaches. The implementation has been done in verilog code. These codes were synthesized and verified using Cadence Encounter RTL compiler tool with geometries at
Crosstalk Delay Avoidance in Long on Chip Buses by using different Fibonacci CODEC Techniques

180nm.

References


Index Terms

Computer Science

Circuits And Systems

Keywords

Crosstalk  Fibonacci  Codec  On Chip Bus