Abstract

Arithmetic Logic Unit (ALU) can be implemented in various ways using different logics. We are proposing an ALU design in which logic gates are implemented using Differential Cascode voltage switching logic (DCVSL). Manchester Carry Chain (MCC) is used to reduce the delay when addition or subtraction is performed in ALU. Using DCVSL logic gates we can obtain complemented outputs without any extra circuitry with zero static power dissipation and rail to rail swing. MCC generates carries parallel to the addition of the inputs, so when adders are
cascaded one stage need not to wait for the carry input from its previous stage. Hence the carry propagation delay is reduced. Proposed ALU can perform all logical operations XOR, XNOR, AND, NAND, OR, NOR and some arithmetic operations like addition and subtraction etc. . .

References


Index Terms

Computer Science
Solid-state Circuits
Keywords
Alu  Dcvsl  Mcc  And  Or  Xor  Nand  Nor  Xnor