Abstract

In this new technology era, circuit partitioning is a fundamental problem in very large-scale integration (VLSI) physical design automation. In this brief, we present a new interconnection oriented clustering algorithm for combinational VLSI circuit partitioning. The proposed clustering method focuses on capturing clusters in a circuit, i.e., the groups of cells that are highly interconnected in a VLSI circuit. Therefore, the proposed clustering method can reduce the size of large-scale partitioning problems without losing partitioning solution qualities. The
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performance of the proposed clustering algorithm is evaluated on a standard set of partitioning benchmarks—ISCAS85 benchmark suite. The experimental results show that the proposed algorithm yields results comparable to that of the rajaraman-wong optimum delay clustering approach with a faster execution time.

References

- Rajmohan Rajaraman and D. F. Wong, "Optimum clustering for delay

Index Terms

Computer Science

VLSI

Keywords

Clustering Benchmark Algorithms Partitioning