Abstract

Flip-Flops are of many types. Choosing the correct type FF for any application is very important to achieve high performance. The data look ahead D Flip-Flop (DLDFF) from the
Comparative analysis of Clock gated Data Look Ahead and Conditional Capture Flip-Flops and their area of Applications family of master-slave type is compared with pulse triggered conditional capture Flip-Flop (CCFF). The effect of clock gating on the performance of these Flip-Flops are analyzed. The two Flip-Flops are compared, with clock gating for power and delay and their field of application is determined. Our simulation results in 0.18µm CMOS technology in HSPICE indicates that DLDFF, for various load values 75% power and 60% delay reduction than DFF due to gating. but Clock Gated CCFF consumes more power on increasing load. Hence for applications that include large load, DLDFF will be the best choice. CGCCFF works well on high frequencies applications with 75% power reduction and 60% higher performance than CCFF. A 8-bit synchronous counter is implemented DLDFF and CGCCFF saves 38% and 15% power consumption on clock gating than DFF and CCFF counterparts. The Pavg obtained for CGCCFF is proved as very much high when compared to DLDFF due to the increased load in counter. Hence it is determined that DLDFF is works well on large circuits and CGCCFF for high frequency applications.

References


Index Terms

Computer Science
Solid State Circuits

Keywords
Clock Gating    Data Look Ahead    Conditional Capture    Young's Architecture    Low Power