Abstract

In the world of Integrated Circuits, Complementary Metal–Oxide–Semiconductor (CMOS) has lost its credentiality during scaling beyond 32nm. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress. As a result of such SCE many alternate devices have been studied. Some of the major contestants include Multi Gate Field Effect Transistor (MuGFET) like FinFET, Nano tubes, Nano wires etc. In this work, the basic gates and memory circuits like DRAM are modeled in HSPICE software using CMOS structure and FinFET structures are analyzed and their performances like standby power Consumption and static noise margin are compared. Also a low power and robust DRAM cells based on FinFET has been proposed for 32nm technology.
Analysis and Performance Comparison of CMOS and FinFET based DRAM Memory Cell

References


Index Terms

Computer Science
Nanoscale Device Modelling

Keywords
Cmos Dynamic Ram Finfet Memory Cell Power Dissipation