Abstract

Voltage Controlled Oscillator (VCO) is an important building block in wireless communication system. In this paper a five stage current starved Voltage Controlled Oscillator (CMOS VCO) is designed which is used in Phase Lock Loop (PLL). The design is implemented on CADENCE VIRTUOSO Platform with high oscillation frequency and low power dissipation. The oscillation frequency of the designed VCO ranges from (665.7MHz-1.128GHz). The circuit is simulated using 180nm CMOS Technology. Simulation result shows that the power dissipation is -12dBm at power supply of 1.8 volt and the phase noise is (-105dBc/Hz @ 10MHz offset). The designing of such VCO shows the efficient performance of the oscillator circuit under given
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conditions. Such design is useful for frequency synthesizer application in PLL with less design
cost.

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Index Terms

Computer Science  Wireless Communication

Keywords

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