Network on Chip a bettering system of System on Chip replacing the traditional bus architectures with Switches and Routers is considered for dynamic reconfiguration. Dynamic reconfiguration of Network on Chip limits the usage of unwanted hardware resources and making the system to work well in varying operating conditions. Though the dynamic reconfiguration reduces the usage of hardware resources and work well in varying operating
conditions, there is an increase in packet loss of the system due to processing core’s
modification by reconfiguration. There have been ideas proposed to dimension the buffer size
for reducing packet loss, meanwhile the throughput and latency gets affected when buffer size
is changed. So a retransmission protocol for recovering the lost packets in the reconfigurable
Network on Chip is proposed here to reduce the packet loss without affecting throughput, and
giving better latency measurements compared to other adaptive Network on Chip.

References

- Berthelot, F. ; Nouvel, F. ; , "Partial and dynamic reconfiguration of FPGAs: a top
down design methodology for an automatic implementation," Emerging VLSI
Technologies and Architectures, 2006. IEEE Computer Society Annual Symposium on , vol. 00,
o., pp. 2 pp. , 2-3 March 2006
- Pionteck, T. ; Albrecht, C. ; Koch, R. ; , "A dynamically reconfigurable
&apos;06. Proceedings, vol. 1, no. , pp. 8 pp. , 6-10 March 2006
- Albrecht, C. ; Koch, R. ; Pionteck, T. ; , "On the impact of buffer size on packet loss
in adaptable network-on-chips for Dynamic reconfigurable system-on-chips," NORCHIP,
- Albrecht, C. ; Foag, J. ; Koch, R. ; Maehle, E. ; , "DynaCORE — A Dynamically
Reconfigurable Coprocessor Architecture for Network Processors," Parallel, Distributed,
and Network-Based Processing, 2006. PDP 2006. 14th Euromicro International Conference on
Reconfigurable Embedded Systems," Design, Automation & Test in Europe Conference &
Exhibition (DATE), 2010 , vol. , no. , pp. 837-842, 8-12 March 2010
- Hossain, H. ; Ahmed, M. ; Al-Nayeem, A. ; Islam, T. Z. ; Akbar, M. ; , "GpNoCsim -
A General Purpose Simulator for Network-On-Chip," Information and Communication
March 2007

Index Terms

Computer Science
Emerging Trends in Technology

Keywords
Fault Injection Automatic Repeat Request-selective Repeat Processing Cores Packet
Transmission Efficiency