A Review of Area Efficient High Speed Multiplier Design

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ABSTRACT
This paper presents the review of high speed multiplier factor style within which the comparison of the VLSI style of the Carry look-ahead adder (CLAA) and also the VLSI style of the Carry select adder (CSLA) supported unsigned multiplier factor. The multipliers styles during this paper were exploitation VHDL (Very High Speed Integration Hardware Description Language) for unsigned information. Here is to planned, the semiconductor style methodologies to higher levels of abstraction and partly to hurry integration, however conjointly to confirm their styles area unit filmable to changes in specifications or system style. In nano scale fabrication of multiplier factor during this paper wee planned a ninety nm multiplier factor style and analysis the performance.

Keywords
Multiplier, Carry look-ahead adder, Carry select adder, VHDL, Modeling & Simulation.

1. INTRODUCTION
With the introduction of nano-scale CMOS technology, analog and mixed styles area unit baby-faced with several new challenges at totally different phases of design. The drift in nano-scale CMOS technologies expected by Moore's law has been fuelled by an enormous demand for ever higher performance and by fierce international competition over the past three decennary. Nano-scale CMOS technology is captivating for many reasons: first Smaller MOSFETs might permit a lot of current to pass, because of their shorter length dimension.

Conjointly MOSFETs area unit like resistors within the on-state, and small resistors have less resistance. Second, smaller MOSFETs have smaller gate areas, and therefore lower gate capacitance. Finally the foremost necessary reason for MOSFET scaling is reduced space, resulting in reduced price as a result of the price per integrated circuits is especially associated with the amount of chips that may be created per wafer. Multipliers area unit unremarkably utilized in varied electronic applications e.g. Digital signal process within which multipliers area unit won't to perform varied algorithms. Computing machine arithmetic is a facet of logic style with the target of developing acceptable algorithms so as to realize an economical utilization of the offered hardware. The essential operations of area unit are division, multiplication, addition and subtraction. In this, we end to area unit reaching to cope with the operation of additives enforced to the operation of multiplication.

2. II. CARRY LOOK-AHEAD ADDER (CLAA)
Carry Look Ahead Adder will manufacture carries quicker because of carry bits generated in parallel by a further electronic equipment whenever inputs amendment. This system uses carry bypass logic to hurry up the carry propagation. A carry-look-ahead adder improves speed by reducing the quantity of your time needed to see carry bits. As shown in figure 1; the computation diagram of carry look-ahead adder calculates one or a lot of carry bits before the total that reduces the wait time to calculate the results of the larger price bits.

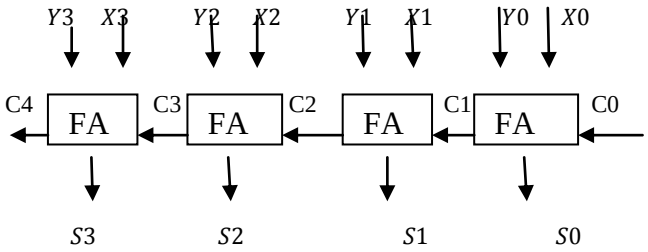

Figure1: Computation diagram of Carry look Ahead Adder

3. CARRY SELECT ADDER (CSLA)
The carry-select adder is straightforward however rather quick. As shown in figure 2; the carry-select adder typically consists of two ripple carry adders and a electronic device. Adding two n-bit numbers with a carry-select adder is finished with two adders (therefore two ripple carry adders) so as to perform the calculation doubly, just once with the belief of the carry being zero and also the alternative presumptuous one. After the two results are estimated, the correct sum and the correct carry are then selected with the multiplexer, once the correct carry is found. The number of bits in each carry select block can be uniform. Generally, to propagate carries multiplexers are used. Because of multiplexers larger area is needed. It has lesser delay as compare to ripple carry adder

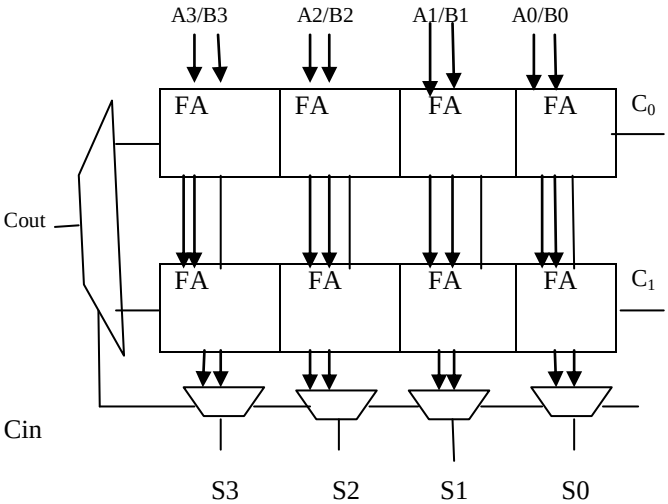

Figure2: Computation diagram of Carry Select Adder

4. CLASSIFICATION OF HIGH SPEED MULTIPLIERS
During this classification as we tend to square measure on planning number we'd like multiplication method. The fundamental principle used for multiplication is to judge partial merchandise and accumulation of shifted partial merchandise.

So as to perform this operation range of serial addition operation is needed. So the most important parts needed to style a number are Adder.

In physical science, associate adder is digital circuit that is employed to perform the addition of binary digits. In VLSI system style victimization adders, we tend to square measure increasing the performance of the module. During this section we'll review the various kinds of adders and their characteristics and performance.

As shown in figure 3; Adders are often Ripple Carry, Carry Look Ahead, Carry select, Carry Skip and Carry Save. Carry Save Adder is employed to try to the summation of or a lot of N-bit of numbers. It is similar as Full Adder. Basically Full adder is a combination of three inputs and two outputs (SUM and CARRY). The Ripple carry adder may be a combination of multiple full adders to feature N-bit numbers. Here we tend to square measure coping with the four-Bit Ripple carry adder. This four-Bit ripple carry adder is that the combination of four full adders. Every full adder has the three binary inputs and two binary outputs add and Carry. Every full adder output Carry is input to consequent full adder this type of adder is termed because the Ripple carry adder. The mainly classified adder's square measure shown below:

All this adders were enforced in their references [10, 11, 14, and 15] victimization completely different technologies supported either computer code implementation work (Viz. VHDL or MATLAB) or hardware implementation work using FPGA implementation of CMOS technology.

1. Carry look-ahead adder (CLAA) is faster but costly adder as compares with other. Its speed is due to computing carry bit i without the waiting for carry bit (i – 1), as define in this paper [11, 15].

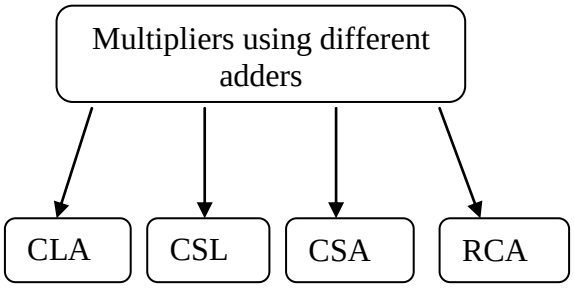

Figure 3: Block diagram of broadly classified adders

2. Carry select adder (CSLA), in this adder the carry find out of each section determines the carry in of the next section, which then choose the suitable ripple carry adder as define in this paper [11].

3. Carry save adder (CSA) in this adder the size of the blocks is chosen or selected so as to minimize the longest life of a carry, as define in this paper [10, 15].

4. Ripple carry adder (RCA), in this ripple carry adder is built when the full adders are cascading in series form as define in this paper [15].

5. LITRATURE SURVEY

During this review analysis the work planned by high speed multipliers victimization carry look ahead adder and carry choose adder for the implementation of multipliers supported space and time.

1. Sertbas et.al [2004] presents the paper on the study of classified binary adder design and also the VHDL simulations. The opposite adders, the carry look ahead (CLA) and also the carry choose (CSLA) adders, behave similar and, have medium space and delay necessities with regard to RCA.

2. P. Asadi et.al [2007] planned the work on highs-speed 54-54 bit number, a brand new 54*54 bit number victimization high speed CLA has been made-up by CMOS technology. This paper presensts a self-timed carry look-ahead adder in which the logic quality was a linearly performs.

3. Raminder Preet Pal Singh et.al [2009] during this paper the planning of two completely different array multiplier square measure given, one by victimization carry-look ahead reason for addition of partial product terminologies and another by introducing Carry Save Adder (CSA) in partial product lines. This work is performed on 32-bit unsigned knowledge. Therefore, it is often extended for signed multiplication.

4. Hasan Krad et.al [2010] planned the work on the performance analysis of 2 completely different multipliers for unsigned knowledge, one uses a carry-look -ahead adder and also the other uses a ripple adder. The paper's mainly examined the speed of the multiplication operation on these 32-bit multipliers that square measure shapely victimization VHDL.

5. N. O. Chintapant et.al [2012], worked on analysis of the representation of different kinds of adders square measure analyzed. This work uses a straightforward and economical gate- level modification to considerably cutback the world and power of the CSLA. Planned style has raised speed and reduced space and power as compared with the regular CSLA with solely a small increase within the delay.

6. V. Vijayalakshmil et.al [2013] given the work on style and Implementation of thirty two Bit unsigned number victimization the CLAA and CSLA. Each of the VLSI style of number multiplies 2 32-bit unsigned whole number values and offers a product term of 64-bit values. This thirty two bit number are often more extended to sixty four bit number and 128 bit number victimization the planned methodology for multiplication operation are often done as future work.

7. Vrushali Gaikwad et.al [2014], in this section, the comparison had shown the idea of multiplier using VHDL this paper presents a highly productive method of multiplication using VHDL. The multiplication using carry save adder is faster and efficient than any other adder.

Table 1. Performance Measures of Multiplier using Adders

S.No	Author Name	Methodology & Implementation	Remarks
1.	P.Asadi et.al [3]	Have utilized CMOS technology and Software tools: for designing a high speed Multiplier using Booth Encoder, Compressor, and CMOS Adder	A 54-54bit CMOS parallel multiplier was proposed to reduce the number of transistor, delay and power consumption. In this, 8.6% improve power consumption and 7.6% reduction in delay.
2.	Radu Zlatanovici et.al	Have utilized the 16 bit full tress Radix (kogge stone & ladner Fischer) for analysis using the Software , CMOS, Adder; CLAA	By analyzing the impact of the main design choices on adder behavior in the energy delay space to reduce the power.
3.	V.Vijayalakhsmi et.al	Have utilized the Array Multiplier for examining the performance of CLAA, CSLA using VHDL Modeling & simulation, Xilinx.	This 32 bit multiplier can further extended to 64 bit and 128 bit multiplier using proposed method for multiplication operations. In this area delay reduce to 31%.
4.	Vrushali Gaikwad et.al	Have utilized the FPGA kit and array multiplier, VHDL for analyzing the parallel multiplier.	This paper presents a method of multiplication using VHDL In this CSA is implemented. This work is Performed on extended 64 bit multiplier.

6. SUMMARY

In this section, the comparison had shown the idea of implementation of multipliers using different adders on different technologies. Array multiplier is commonly known for its regular structure. Its circuit is mainly based on add and shift algorithm. By multiplying the multiplicand with single multiplier bit each partial product is generated. According to their bit position the partial product are shifted and added. The addition operation is done by a common carry propagate adder. A total of N-1 adders are needed where 'N' is the length of multiplier. The final multiplication product is attained in the last adder by using any fast adder like carry ripple adder. In this type of multiplication we need to add each and every partial product as there are multiplier Array number is usually familiar for its regular structure. Its circuit is principally supported add and shift formula. By multiplying the number with single number bit every partial product is generated. The addition operation is completed by a typical carry propagate adder. A complete of N-1 adders area unit required wherever 'N' is that the length of number.

The final multiplication product is earned in the last adder by victimization any quick adder like carry ripple adder. During this style of multiplication we want to feature each and every partial product as there area unit number bits. The most disadvantage of the array number is that the delay in computation with relation to the dimension of the number.

Hence, the speed of the number is low additionally the general Power consumption and space is low.

This formula works by reducing the quantity of partial product thereby pressing the adder tree. Shift-and-add multiplication is same as that of basic multiplication performed mathematically. During this methodology the number 'A' is intercalary to itself 'B' times, wherever 'B' is the number. Mathematically to multiply two numbers, the formula is to require the only digit of the number from right to left one at a time. Then, the number is increased by a single digit of the number and the obtained intermediate product is placed to the left of the past results in separate positions. For playacting the complete operations to get the Quotient, the standard design for shift and add multipliers bear several switch activities. as a result of these switch activities the dynamic power consumption is high in typical design. so as to cut back the switch activity in the typical number design, low power design will be designed. In this paper we tend to have projected a changed Universal Shift register primarily based shift and add number with reduced dynamic power consumption.

Power and delay estimation: to live power and delay for the finished number layouts–including the delay and capacitance of all the inter-cell wiring. Cell characterization: to know power consumption in every of those primitive element cells, as enforced by typical static CMOS circuits. Layout model, to permit exploration and first-order estimation of wiring, delay and space, we want an easy layout vogue that's simply automatable, nevertheless not thus elaborated on demand manual, full-custom layout. During this section performance measures of multipliers mentioned up to now area unit summarized and compared.

From the Table I. we are able to see that delay of Wallace tree number and Combined Booth-Wallace tree number is nearly constant and is that the least. In this analysis [11], the delay time is nearly same, the area and the area delay product of CSLA based multiplier is reduced to 31% when compared to CLAA based multiplier. The CLAA based multiplier delay (ns) is 98.5, Area 2957 logic cells and Delay Area Product is 291264.5 and CSLA based multiplier delay (ns) is 99.5, Area is 2039 logic cells and Delay Area Product is 2028805.using CSLA improves the overall performance of the multiplier. On comparison of carry look-ahead adder (CLAA) based multiplier the area of calculation of the carry select adder (CSLA) based multiplier is smaller and better with nearly same delay time. This paper deals with the comparison in the bit range of n*n (32*32) as input and 2n (64) bit output. Hence, to design a better architecture the basic adder blocks must have reduced delay time consumption and area efficient architectures.

7. PROPOSED METHODOLOGY

Multiplication is one in every of the fundamental arithmetic operations. Multiplication operation is additionally known as a adding and shifting methodology. Multiplication operation involves 2 strategies one is Generation of partial product and another one is summation. The speed of multiplication is

principally depends on the Partial product generation and/or summation. The multiplication speed is going to be high once the generation of partial product is a smaller amount. In this, we tend to area unit aiming to implement the 2 32-bit unsigned multipliers victimization adders. In several processors Carry select adder is employed to perform the quick arithmetic operations. The carry propagation delay time is incredibly high in Ripple carry adder. To beat this downside Carry look-ahead adder is projected. This sort of adder doesn't need the carry propagation step by step.

8. CONCLUSION

This work evaluates the performance of the projected styles in terms of delay, speed (frequency) and memory. The results analysis shows that the projected CSLA structure is best than the regular CSLA. And it's enforced in number as application for economical performance. Performance analysis of varied Adders is analyzed in terms of delay, frequency and memory from these carry choose adder is best parameter values than alternative adders. And therefore the regular carry choose is additional changed for speed and space potency. The projected style that changed carry choose adder having higher speed than regular carry choose adder and space additionally reduced .by this design the economical number designed. Finally, the fascinating continuation of this work is to analyze the opposite binary adder architectures and to increase to the performance comparisons for the all adder structures.

9. REFERENCES

[1] P. Asadi and K. Navi, "A novel highs-speed 54-54 bit Multiplier", Am. J Applied Sci., vol. 4 (9), pp. 666-672. 2007.

[2] W. Stallings, Computer Organization and Architecture Designing for Peljormance, 71h ed., Prentice Hall, Pearson Education International, USA, 2006.

[3] 1. F. Wakerly, Digital Design-Principles and Practices, 4th ed., Pearson Prentice Hall, USA, 2006.

[4] A. Sertbas and R.S. Ozbey, "A performance of classified Binary adder architectures and the VHDL simulations", Electronics Engineering Istanbul, Turkey, vol. 4, pp. 1025-1030, 2004.

[5] P. S. Mohanty, "Design and Implementation of Faster and Low Power Multipliers", Bachelor Thesis. National Institute of Technology, Rourkela, 2009.

[6] S. Brown an111d Z. Vranesic, Fundamentals of Digital Logic with VHDL Design, 2nd ed., McGraw-Hill Higher Education, USA, 2005. ISBN: 0072499389

[7] J.R. Armstrong and F.G. Gray, VHDL Design Representation and Synthesis, 2nd ed., Prentice Hall, USA, 2000.

[8] Z. Navabi, VHDL Modular Design and Synthesis of Cores and Systems, 3rd edition, McGraw-Hill Professional, USA, 2007.

[9] Hasan Krad and Aws Yousi("Design and Implementation of a Fast Unsigned 32-bit Multiplier Using VHDL", 2010

[10] Raminder Preet Pal Singh, Parveen Kumar, Balwinder Singh, "Performance Analysis of 32-Bit Array Multiplier with a Carry Save Adder and with a Carry-Look-Ahead Adder", International Journal of Recent Trends in Engineering, Vol 2, No. 6, November 2009.

[11] V.Vijayalakshmil, R.seshadri, Dr. S. Ramakrishnan , "Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA",IEEE-2013.

[12] P. C. H. Meier, R. A. Rutenbar and L. R. Carley,"Exploring Multiplier Architecture and Layout for low Power", 1996

[13] Navi.K, Kavehei.O, Rouholamini.M , Sahafi.A, "Low-Power and High-Performance 1-bit CMOS Full.Adder Cell,"Journal of Computers, Academy Press, vol. 3, no. 2, Feb. 2008.

[14] Rajender Kumar, Sandeep Dahiya, "Performance Analysis of Different Bit Carry Look Ahead Adder Using VHDL Environment, International Journal of Engineering Science and Innovative Technology (IJESIT)", Volume 2, Issue 4, July 2013

[15] Vrushali Gaikwad, Rajeshree Btramankar, Amiruna Warambhe"32 bit parallel multiplier using VHDL" International Journal of Engineering Trends and Technology (IJETT)", Volume 9, Issue 3, March 2014