

FPGA – based High Resolution Digital Pulse Width Modulator with Minimum Sequential Reset Logic

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ABSTRACT

Digitization of modern world has led to increasing use of digital equipment. The pioneer equipment in this regard is Digital Pulse Width Modulators. Although there is limit on clock frequency which is to be used in digital circuit. This paper describes simple Digital Pulse Width Modulator with optimized Area using Field Programmable Gate Arrays (FPGA). The proposed architecture uses a phase shifter mechanism provided by on chip Digital Clock Manager (DCM) in FPGA. The circuit uses such design to reduce cell Area to greater limit. The design is experimentally tested and compared with other design.

Keywords

HRDPWM, DCM, FPGA, RESET logic

1. INTRODUCTION

The recent shift in control techniques used in power converters [2] from conventional analog control to more advanced and deeply examined digital control was seen due to the many advantages digital control offers and including the following.

Workability: Control is implemented by writing a programming code which can be easily changed without changing the complex hardware. It is not like the using discrete components like resistors and capacitors used to control while using analog techniques.

Reliability: Digital control allows an environment free from component by using a fast and highly reliable, power-efficient and compactly integrated microprocessor. This is totally different from analog control where various discrete components are used. Dense integration with few components which implies reduced failure of design making it nearly free from environmental changes, aging and temperature variations and thus increasing the overall reliability of digital control design.

On the contrary, analog control is free from terms like resolution and sampling without which digital control is impossible. Thus, the digital control apart from providing almost noise free environment and advantages listed above has added ambiguities in the form of limited resolution and added delays [3] [10] due to sampling and other processing technique leading to degraded accuracy.

For control mechanism almost all embedded system uses pulse width modulators (PWMs) [4]. Therefore a large number of PWM architectures had been proposed [5] [7]. Among these PWM architectures Digital Pulse Width Modulators (DPWM) are extremely popular. It has become an integral part of a large number of electronic appliances. One of the prominent applications of DPWM lies in power electronics for controlling pixels in HDTV. Picture elements

are one of those which extensively use concept of PWM for its operation. Output of PWM circuits is a square waveform whose turn on time or turn off time is varied. A unique term is defined in relation to pulse width modulator output called Duty Cycle. The duty cycle is the ratio of on time (TON) to total time period (T) of signal. The simple PWM diagram describing the concept of duty cycle is shown in figure.1.

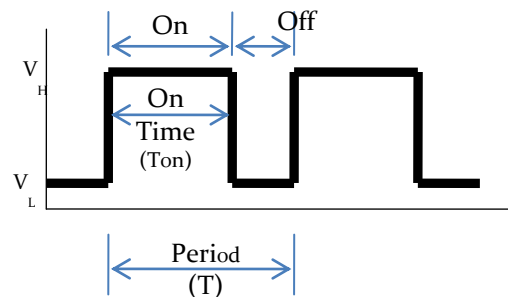


Fig.1 PWM waveform depicting ON/OFF time

It is expressed in (%) as,

$$\% \text{ Duty Cycle} = \frac{\text{On Time}}{\text{Total Period}} \times 100$$

This ratio can vary from 0 to 100 percentage depicting pulse width modulated output. Average signal level can be found as:

$$V_{avg} = D \cdot V_H + (1 - D) \cdot V_L$$

Usually, V_L is taken as zero volts for simplicity.

The circuits previously published used a lot of sequential logic for delaying the reset signal resulting in a large part of cell area of FPGA been used for implementation. The aim of this paper is to use minimum sequential logic as far as possible in order to decrease the cell area used in FPGA to greater limits. Moreover, use of minimum sequential logic will also result in reduction of overall power in DPWM architecture, providing a more convenient final implementation. Our proposed architecture thus can allow working the circuit at higher efficiency.

This paper is organized as follows. Section 2 describes the proposed High Resolution Digital Pulse Width Modulator using minimum sequential reset logic. The Xilinx implementation details are explained in Section 3. The results of proposed architecture in Xilinx tool and Synopsys tool is shown in Section 4. Finally, the main conclusion of the work is drawn in Section 5.

2. RDPWM WITH MINIMUM SEQUENTIAL RESET LOGIC

2.1 Conventional Previous HRDPWM Architecture

HRDPWM [1] [8] architecture is divided in different stages namely, 1) Phase Shifter Stage, 2) Counter and Comparator Stage, 3) RESET Stage, 4) On-Off Stage.

1) Phase Shifter Stage: Although there are many Phase Shifter Stage architectures [9], HRDPWM Phase Shifter Stage uses the on board DCM i.e., Digital Clock Manager Present in FPGA [6]. FPGA offers maximum of 4 on board DCM at a time. DCM Provides following operation:

- Fixed Phase Shifted Clock Output.
- Variable Phase Shifted Clock Output.
- Multiplication/Division of Clock.

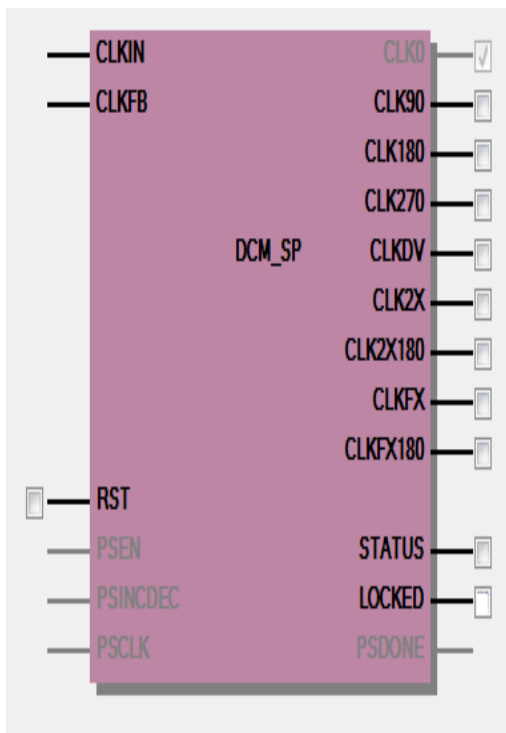


Fig.2 IP core generated on board DCM in FPGA

The conventional previous architecture uses clkIn, clkfx pin as shown in Fig.2 of on chip DCM to provide input and multiplied clock output respectively. For providing phase shift operation it uses clkIn as input and clk0, clk90, clk180, clk270 as output pin as shown in Fig.2 to provide phase shifted output of 0, 90, 180, 270 through respective pin. In addition to phase shifted output from DCM pin, it can also provide phase shift operating in its either fixed or variable phase shift mode. The proposed architecture uses fixed phase shift mode of operation of DCM.

2) Counter and Comparator Stage: DPWM uses a counter usually an up/down counter to count either at the rising or falling edge of clock. The counter output is fed to comparator for comparison with the data provided by user. The comparator then generates two output signals to be used by reset logic and on/off stage used in the architecture. It is to be noted that as soon as the counter counts reaches the same value fed by user, the comparator output will set.

3) RESET Stage: This stage performs the main function of DPWM that is to control the width of DPWM according to data given by user/devices. The architecture used a Synchronous circuit to reset the pulse as shown in figure.

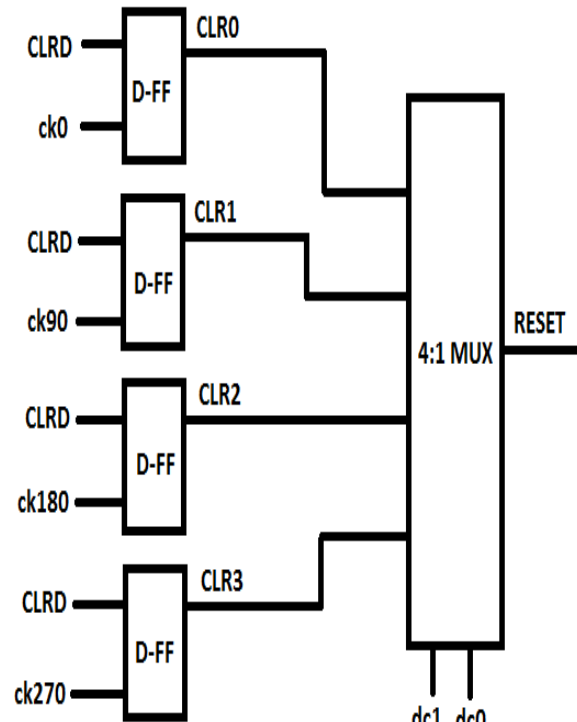


Fig.3 RESET logic used in Conventional HRDPWM Architecture

From above Fig.3 it is clear that four D flip-flop are fed with phase shifted output of 0, 90, 180, 270(in degrees) generated by DCM at their clock inputs. Data in input of D flip-flop is fed with comparator output which get set (as discussed above). It is shown by CLR0, CLR1, CLR2, CLR3. These are then fed at the input of 4:1 MUX. According to data given by user at the select input pin of 4:1 MUX one of the four input of 4:1 MUX is used to set the output of MUX.

4) On-Off Stage: Single stage SR flip-flop is used to govern on as well as off time of the pulse generated by HRDPWM. The architecture utilized all three states of SR flip-flop. These states are: a) when set input terminal is at logic high, b) when reset input terminal is at logic high, c) when both set and reset terminal are at logic low level. This means that the SR flip-flop is always operated in between these three states. Till the counter count was less than the input given by user the set input terminal of SR flip-flop was at high logic enabling the pulse output to be at logic high. The time up to which pulse output will be at logic high is termed as ON period of pulse. As counter count reaches the input given by user the Reset Stage of the architecture set the reset terminal of SR flip-flop at logic high level enabling the pulse output to be logic low. The time up to which pulse output will be at logic low is termed as OFF period of pulse. The sum of ON period and OFF period will be exactly equal to time taken by counter to reach maximum count.

2.2 The Proposed Modification in RESET Stage

The RESET Stage is redesigned using Minimum sequential circuit elements. One such circuit element which matches the requirement to be used as RESET Stage in HRDPWM is AND gate. The function of D flip-flop used in previous architecture is to generate clear signal. This clear signal is generated when comparator output CLRD is set. The network of D flip-flop whose clock inputs are fed with phase shifted output from DCM then passes the CLRD signal from comparator at the edge of these phase shifted output from DCM. Clear signal generated by network of D flip-flop is then selected by a multiplexer to be used to generate a signal which is used by reset terminal of SR flip-flop to govern turn-off of the pulse. In much the same way AND gate mixes the phase shifted output from DCM with that of CLRD output generated by comparator. It is to be noted that AND gate will generate output (Logic HIGH) only when comparator output CLRD is high which is same as generation of clear signal from D flip-flop only when CLRD Signal from comparator goes high. As such D flip-flop's used in previous architecture are replaced with AND gates. The input to AND gates remains phase shifted clock signal from DCM and the comparator output. Replaced AND gate in place of D flip-flop is shown in Fig.4.

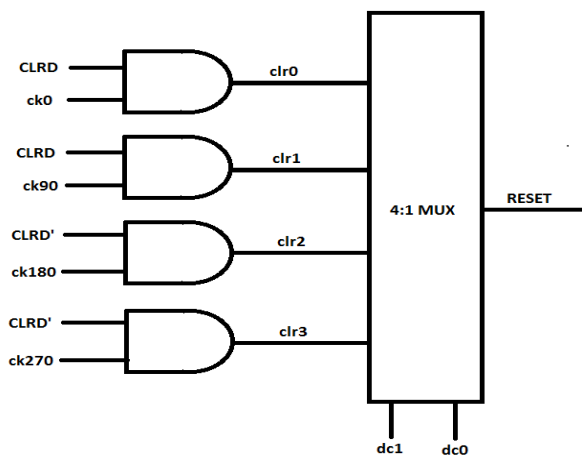


Fig.4.a

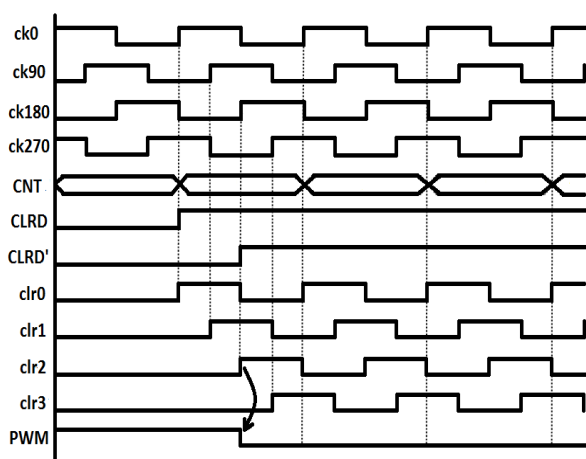


Fig.4.b

Fig.4.a Proposed Modified RESET logic with minimum sequential element and Fig.4.b its waveform

From Fig.4.a and Fig.4.b it is clear that one of the input to AND gate are ck_0 , ck_{90} , ck_{180} , ck_{270} as phase shifted clock output from DCM. Whereas the second input of first two AND gates is CLRD and for other two AND gates it is CLRD'. CLRD is an output signal from comparator. Whereas CLRD' is an output from comparator phase shifted by 180 (degrees). This is done to generate clr_0 , clr_1 , clr_2 , clr_3 with a progressive phase shift of 90(degrees) from each other and to make output from AND gate with one of input ck_0 to be easily differentiated with output from AND gate with one of the input ck_{180} . Similarly, to differentiate between output of AND gate with input ck_{90} and output of AND gate with input ck_{270} , CLRD' is given as another input to AND gate with input CK_{270} . Avoiding CLRD' will lead to clr_0 of AND gate with input ck_0 and clr_2 of AND gate with input ck_{180} non-differentiable at reset terminal of SR flip-flop.

Similarly, clr_1 will be non-differentiable with clr_2 at reset terminal of SR flip-flop. To eliminate this problem CLRD need to be shifted by 180 (degrees) before being fed as input to AND gates with input ck_{180} and ck_{270} . This is done by using a D flip-flop. CLRD is fed as input to D flip-flop whose clock input is fed with ck_{180} from DCM to generate CLRD' as shown in Fig.5.

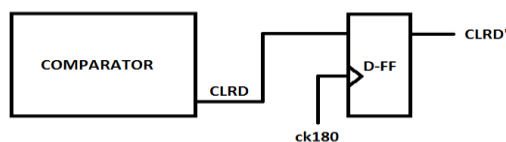


Fig.5 Generation of CLRD' used in Proposed modified architecture

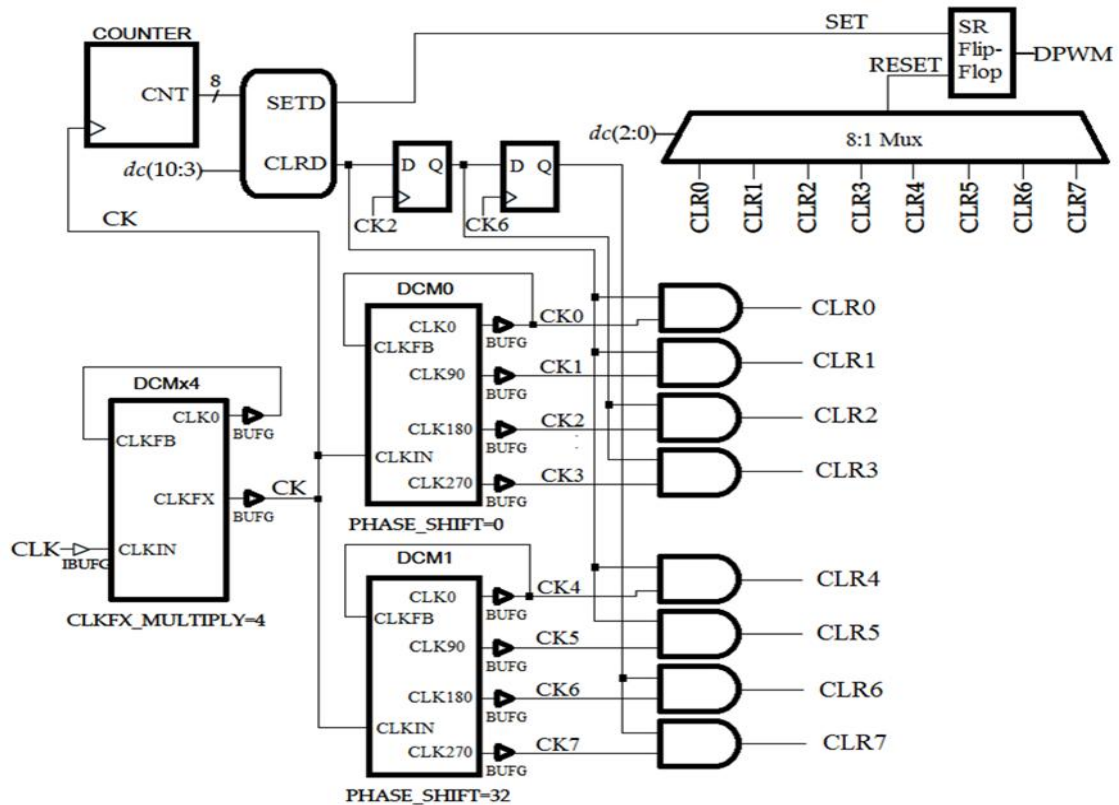


Fig.6 Block Diagram of 8-bit Modified HRDPWM synthesized in Xilinx tool

3. XILINX IMPLEMENTATION OF PROPOSED ARCHITECTURE

HRDPWM with Minimum sequential RESET Stage is implemented in Xilinx tool. Its block diagram is as shown in figure above. Fig.6 as shown above is Proposed Architecture (8-bit) as synthesized in Xilinx tool. Three on board DCM's are used in design. First DCM is used in clock multiplication mode. It is used for multiplying clock by a factor of four. Two other DCMs connected in parallel are used for producing phase shifted output. Among these two DCMs, one of the DCM is operated in fixed phase shifting mode of 32/256 of

time period of clock. Phase shifted output from DCM are then applied as input to network of AND gate. Other input to AND gates are fed with comparator output and phase shifted comparator outputs. Comparator output or phase shifted comparator output together with phase shifted output from DCM are used to generate clear signal (clr (7:0)). This clear signal is then selected by 8:1 multiplexer by using select input terminal of multiplexer. Control of select input terminal of multiplexer is user dependent. Selected clr signal from multiplexer is then fed to reset input terminal of SR flip-flop. As soon as reset terminal of SR flip-flop is at logic high level, it will switch the pulse width modulated output off.

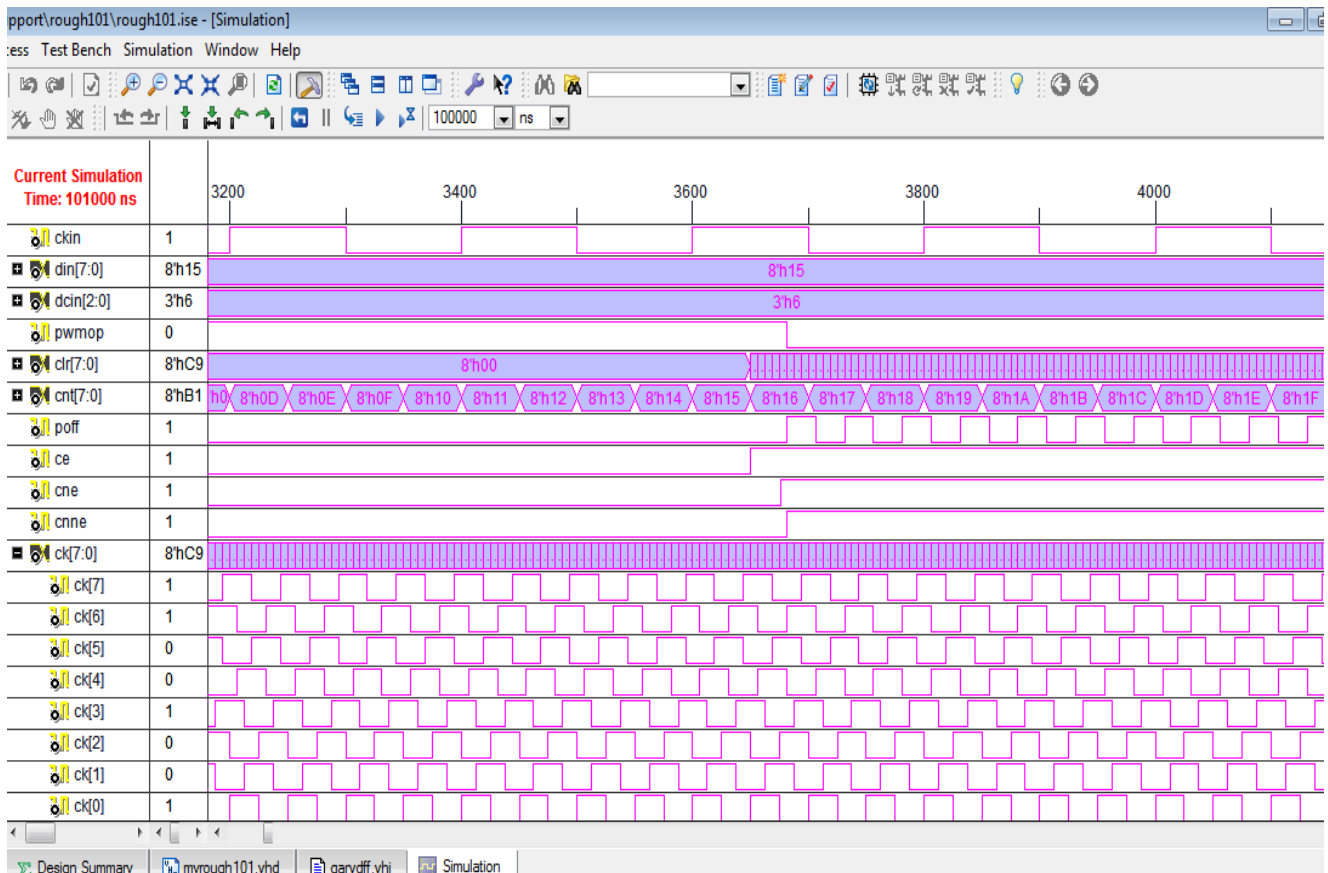


Fig.7 Modified HRDPWM simulated in Xilinx Tool

After HRDPWM with minimum sequential reset stage is synthesized, it is verified using ISE simulator in Xilinx as shown in Fig.7. Simulation is carried out at behavioral level. To simulate the architecture, new source is added to main architecture which contains the test bench or the behaviour of test bench used to check functioning of main architecture. Test bench can be applied in Xilinx in two ways. One way is to directly draw test bench waveform in Xilinx. This waveform is then saved as .vhw extension. Another method is to write the behaviour of test bench waveform required to verify design as VHDL code. This behaviour of waveform is then saved as .vhd extension. Either of the waveform extension file is then applied to modified architecture as new source. Simulating the architecture then gives the timing diagram of the behaviour of VHDL code of modified architecture. This timing diagram is then used to verify the working of proposed minimum sequential RESET logic.

4. RESULTS

The proposed DPWM architecture is implemented in Xilinx using General purpose product category, Spartan 3E family, XC3S250E device having TQ144 package. Out of available speed of -5 and -4, the architecture used speed of -4. Table1 shows the results obtained after the synthesis of proposed architecture and Conventional HRDPWM Architecture in Xilinx tool .

Table1. Synthesis Result obtained for Proposed Modified Architecture and Conventional HRDPWM Architecture

Logic Utilization	Used as in Proposed Modified Architecture	Used as in Previous Conventional HRDPWM Architecture
Number of Slices	12	19
Number of Slice Flip Flops	11	22
Number of 4 input LUTs	23	29
Number of bonded IOBs	13	13
Number of GCLKs	10	10
Number of DCMs	3	3

From Table1 it is clear that number of slices, number of slice Flip Flops and Number of 4 input LUTs have reduced significantly. It is due to minimum sequential reset logic used in proposed modified architecture. In this architecture instead of D Flip-Flop combinational logic i.e. and gate is used as such D flip-flop which itself is composed of number of and gate which results in reducing the sequential logic.

Power and Area estimation of proposed architecture is carried out in Synopsys tool and the result obtained is shown in Table3

Table2. Estimated Area and Power for proposed modified and conventional HRDPWM Architecture

Parameter	Values obtained in Proposed Modified Architecture	Values obtained in Previous Conventional HRDPWM Architecture
Total cell Area	180.00	299.00
Power(in μ W)	9.3216	12.7006

From Table2 it is clear that values of power and area as obtained in Synopsys tool for proposed modified architecture is less than previous conventional HRDPWM architecture. This reduction in power and area can be attributed to minimum sequential reset logic used in proposed modified architecture.

5. CONCLUSIONS

The work has shown implementation of HRDPWM with minimum sequential RESET logic. The architecture is well tested in Xilinx tool. Verification of various parameters is carried out in Xilinx tool. For Power and Area estimation Synopsys tool is used. Minimum sequential RESET logic allowed a significant reduction in cell area (180.00) used in FPGA and a small reduction in power (9.3216 μ W) which is enough to show overall feasibility of the architecture. This modulator architecture can be used in number of application efficiently like generation of picture element for HDTV. Moreover, future work in this architecture can be carried out for reducing overall delay in the architecture.

6. REFERENCES

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