5 Hz Cut-Off Frequency Low Power Current Mode Low Pass Filter

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ABSTRACT
A current mode low pass filter is presented, using current mirror active element. in proposed scheme time constant is increased by increasing capacitance & resistance. Capacitance is increased by capacitance multiplier. Resistance is increased by very low trans-conductance which is achieved through linear compression of input signal. To preserve gain of the system, expansion is done at the output level. To increase current gain and output impedence cascode stage is used at the output branch. All the results are simulated using ANALOG DESIGN ENVIRONMENT OF THE CADENCE SOFTWARE at 180nm CMOS technology.

General Terms
LPF, capacitor multiplier, current mirror.

Keywords
Gain, BW, power, THD, input referred noise.

1. INTRODUCTION
Biological signals are ranged at low frequencies. To separate out these signals from noise or other undesired signals low pass filter with a very low bandwidth is required. Low pass filters can be designed using either passive elements or active elements. Active filters are more attractive in ICs fabrication. Active filters are voltage controlled and current controlled. active filters are designed using op-amp or differential circuit or current mirror or current conveyor etc.

Current mirrors are attractive cell in filter designing with their more simple structure. They provide capability for implementing filters with low power dissipation, low voltage, wide swing , high gain. The current-mirrors are feasible for biomedical applications only when they are capable for realization of large-time constants circuit. time-constants are given by the expression T = C/gm, where gm is the small-signal trans-conductance of the input MOS transistor which is dependent on the bias current Id, the large time-constants can be achieved by increasing the value of capacitance and/or reducing the value of trans-conductance through the bias currents.

With regards to the 1st solution, capacitance multipliers have been already introduced in [2–4]. The solution in [3] is based on the current-mirror as active element, while solutions in [4,5] the active elements are Operational Trans-conductance Amplifiers(OTAs) and/or second generation Current Conveyors (CCIIs). Thus, in terms of simplicity the scheme in [3] is the most preferable.

Reduction in trans-conductance can be done by reducing the bias current i$_d$. In current mirror filters, the input current

should be smaller than the bias current (i.e. I$_{in}$≤ Io). Therefore, this solution limits the range of the input currents which could be handled by the filter.

In order to overcome the above mentioned difficulties, an alter-native solution for realization of large time-constants is presented in this paper. According to this, capacitance multipliers and a scaling of the trans-conductance used for realization of the large time-constant is performed without restricting the range of the input currents. These have been achieved through the employment of appropriate linear compression and expansion of the input and output currents, respectively. This paper is organized as follows: the proposed scheme is presented in Section 2, while its performance is evaluated and compared with that offered by the conventional topology in Section 3, using the Analog Design Environment of the Cadence software and the Design Kit of the TSMC 180 nm CMOS process.
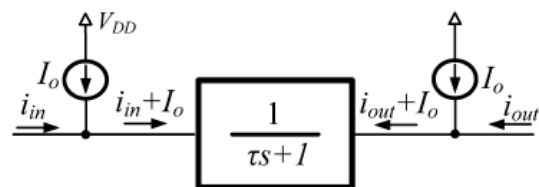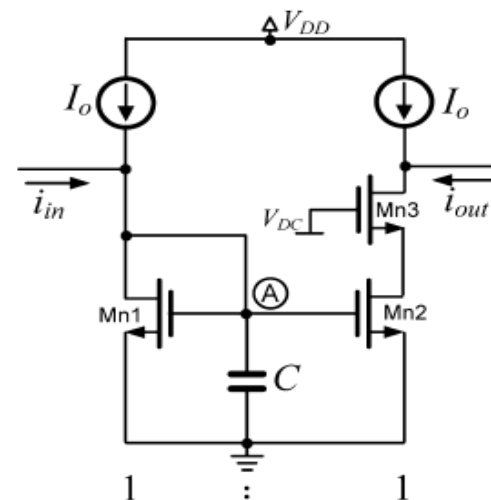

Fig. 1 Core of the filter

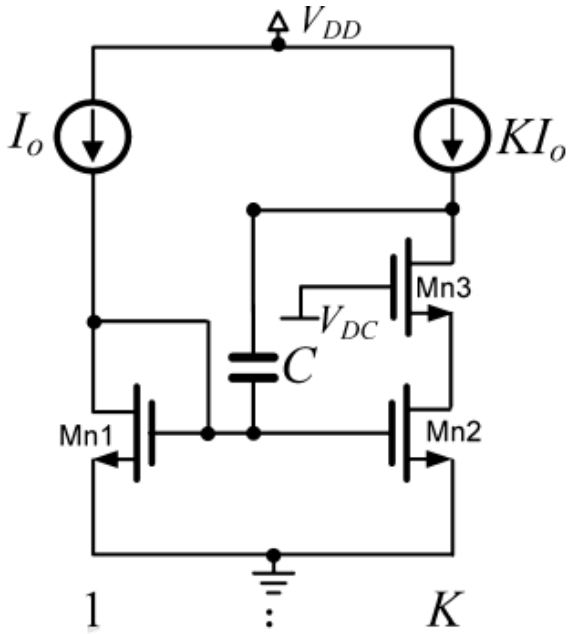**Fig. 2 Ist Order CMOS current mirror filter**

Fig. 1 Capacitor multiplier filter introduced in [2]

2. PROPOSED SCHEME FOR REALIZATION OF LARGE TIME-CONSTANTS IN CURRENT-MIRROR FILTERS

A typical Functional Block Diagram (FBD) of a current-mode 1st-order low pass filter is depicted in Fig. 1 A possible realization using current-mirrors as active elements is demonstrated in Fig. 2 and the ac transfer function is given by (1)

$$\frac{iout}{iin} = \frac{1}{1 + \tau s}$$

The variable τ, in the equation, is a time constant, is given by,

$$\tau = \frac{c}{gm}$$

Where gm is the small-signal trans-conductance parameter. Assuming operation of the transistors in the sub-threshold region and the expression of time constant is given by,

$$\tau = \frac{nVC}{I},$$

Where n is the sub-threshold slope factor (1 < n < 2), VT is the thermal voltage (=26 mV at 27◦C), and I is the bias current. According to (3), large time-constants could be realized by increasing the value of capacitor through a capacitance multiplier and/or reducing the value of trans-conductance by a factor K. The capacitance scaling introduced in [3] is depicted in Fig. 3, where a multiplication of the capacitor value is given by a factor (K + 1). The corresponding filter topology suitable for realizing large time-constants would be more complicated than that in Fig. 2, because the capacitor would be substituted by the scheme in Fig. 3. In addition, the dc power dissipation of the filter in Fig. 2 is 2 Vdd Io, while the corresponding value for the scheme with capacitor scaling would be significantly increased to a level(3 + K)V_{DD}I.

As current decreases, trans-conductance increases which results in increased time constant but input swing decreases in the same manner which is not a feasible solution.

To overcome these above mentioned problems the input current is linearly compressed before applying to the basic current mirror, results in increased time constant .this processed current is then applied to the cascode circuit which causes expansion of the compressed current using large current gain of the cascade circuit. Cascade circuits also provide large output resistance. The current-mirror filters are attractive elements for realization of ultra-low power filters suitable for handling extremely low frequency signals.

The circuitry that implements the FBD in Fig. 4 is given in Fig. 5. The current that feeds in transistor Mp1 is (i_{in} + Io) while, due to the current mirror formed by transistors Mp1−Mp2, the current in transistor Mn1 will be equal to (Iin+ Io)/K. Thus, a linear compression of the instantaneous value of the input current is obtained. both the dc (Io) and ac (Iin) components of the input current are compressed then, the value of trans-conductance of Mn1 is decreased by a factor of K. the reali.zed value of time-constant is increased by the same fact.

It should be also mentioned that the amplitude range of the input current is determined by the level of dc bias current (Io) and this is not affected by the proposed solution. In other words, an orthogonal adjustment between the achieved scaling factor and the level of the maximum current that could be handled by the filter is achieved and this is very important from the flexibility point of view.

Power consumed by the proposed circuit design is (2+1/k)VddIo, which capacitor multiplier circuit LPF design is (3+k)VddIo . Proposed circuit is more attractive into the vie of complexity and the power dissipation.

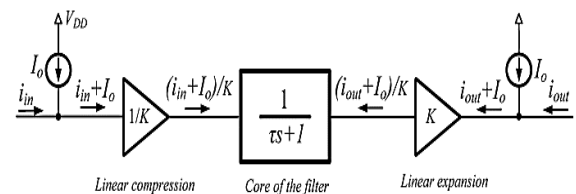**Fig. 2 Proposed core filter**
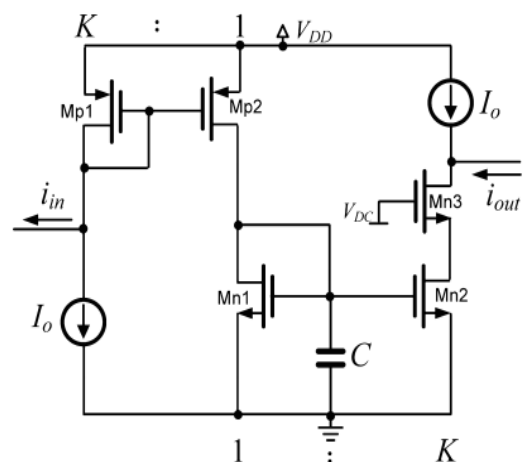

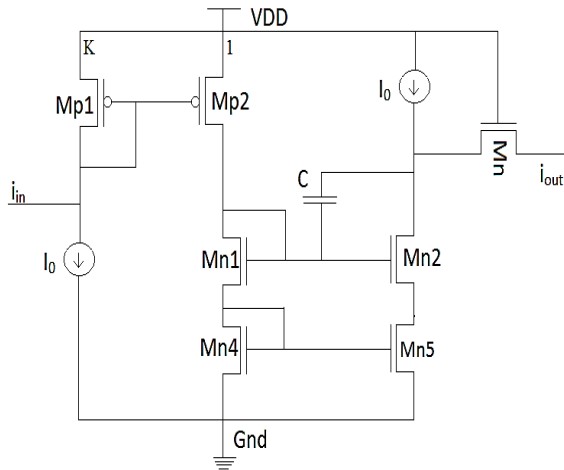**Fig. 3 Large time constant filter**

Fig. 4 Proposed CMOS low pass filter with large time constant

3. SIMULATION AND COMPARISON RESULTS

The performance of the filter in Fig. 6 has been evaluated using the Analog Design Environment of the Cadence software and the Design kit provided by UMC 180 nm CMOS process. The employed dc bias voltage scheme was VDD= 0.5 V, while the dc bias current was Io= 1 nA. In order to realize a low pass filter with cut-off frequency fo= 5.05Hz, the required capacitor value will be equal to 2 nF. From the integration point of view this value is non-realizable. In the proposed solution, the required time-constant could be realized by a capacitor equal to 40 pF and a scaling factor of trans-conductance K = 3. The aspect ratios of transistors were 500nm/500nm for Mn1, 500m/500nm for Mn3, and 500nm/500nm for Mp2. The distribution of dc current has been performed using n-MOS and p-MOS current mirrors respectively. The simulated frequency responses of the filter in Fig. 6 for c= 17.5, 32.5and 40 pf are provided in Fig. 7, demonstrating the electronic tuning capability of the filter. The cut-off frequencies were 11.5 Hz, 6.22Hz, and 5.05 Hz, respectively. The linear performance of the filter in Fig. 8, obtained through the Periodic Steady State (PSS) analysis of the Analog Design Environment, is depicted in the plot where it is obtained that a Total Harmonic Distortion (THD) level equal to 2% is achieved for amplitude of the input signal equal to -50dbm.out put power gain for pout(dbm) -50, -40, -30,-20 and -10 dbm are 115, 105, 95, 85 and 75 db respectively. AC analysis of this scheme gives gain 5.5db . average values of input squared noise is 0.439pA.

Table 1 Comparison results for filters

Performance factor	Fig5	Fig6
Power(nW)@ V_{dd}= 0.5v	3.05	2.5
Amplitude(dbm)@2%THD	-55	-45
input referred noise in rms	0.47pA	0.43pA
Dynamic range (db)	64.7	83.29
Cut-off frequency, f_o Hz	10	5.056

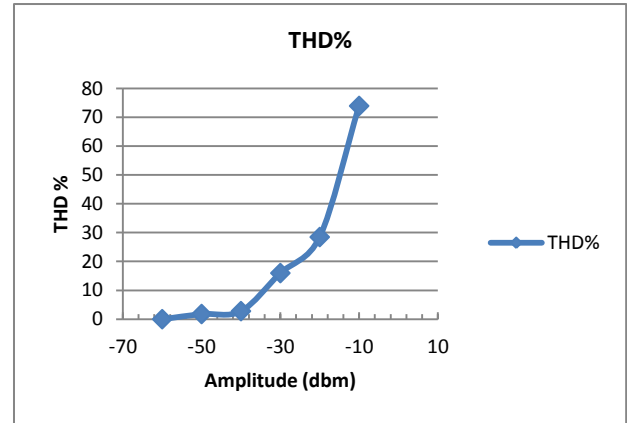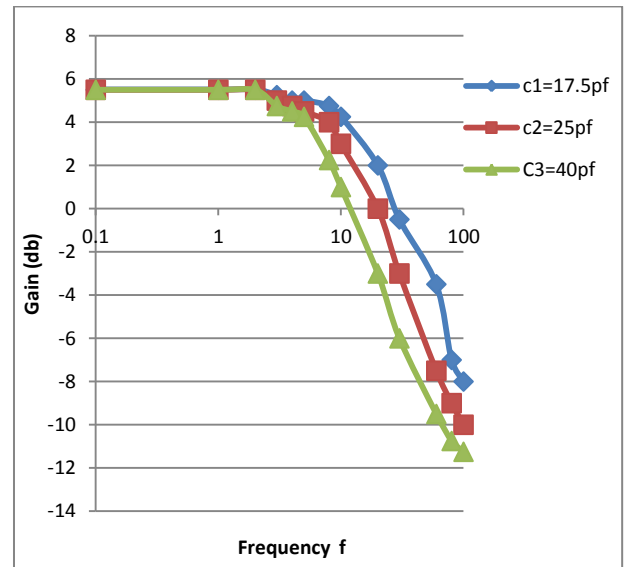|		
Capacitor value pf	47.4	40
Gain(db)	0	5.5

Fig7 THD plot

Fig8 gain plot

4. CONCLUSION

Proposed circuit is more linear in terms of total harmonic distortion. Dynamic range of this scheme is better than conventional cmos filter. Cut-off frequency is 5.05Hz at small capacitance value 40pf which require small area on chip fabrication. This scheme also provides electronic tuning with variation in I_O. proposed circuit has gain 5.5db more than conventional circuit. Power dissipation of proposed circuit is less than conventional. Therefore, it is an attractive scheme for implementing biomedical signal processing systems with tunable LPF with on-chip capacitors. This work can be extended for higher order filters using ladder structure technique. Higher order filter shows sharp cut-off frequency than single order filter.

5. REFERENCES

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