

# Static Power Reduction in 32-bit Ripple Carry Adder using Dual Threshold Voltage Assignment

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## ABSTRACT

Reduction in leakage power has become an important concern in low-voltage, low-power, and high-performance applications. In this paper, the dual-threshold technique is used to reduce leakage power in a 32-bit ripple carry adder by assigning high-threshold voltage to some transistors in noncritical paths, and using low-threshold transistors in critical path. The circuit was implemented using Cadence Virtuoso tools in 90-nm technology. The optimized layout of the ripple carry adder is designed using Cadence Virtuoso Layout Suite. Performance parameters such as total power, delay, static power and power delay product (PDP), were calculated and compared with the existing design topologies of full adder. The simulation results of the 32-bit ripple carry adder using the dual threshold voltage technique are compared with the conventional 32-bit ripple carry adder with different threshold values. Results show that the dual-threshold technique is good for leakage power reduction during runtime mode.

## General Terms

CMOS, full adder, ripple carry adder, critical-path, delay, high performance, low-power design, low voltage, power estimation, layout.

## Keywords

Leakage power, static power

## 1. INTRODUCTION

With the growing use of portable and wireless electronic systems, reduction in power consumption has become more and more important in today's very large scale integration (VLSI) circuit and system designs [2],[7].

In CMOS digital circuits, power dissipation consists of dynamic and static components. Of the two sources of power dissipation in CMOS circuits, aggressive device feature size scaling leads to reduction in per transistor dynamic power dissipation. As dynamic power depends quadratically on the supply voltage  $V_{dd}$  and static power is directly proportional to it, supply voltage reduction has the most profound effect on power consumption of CMOS circuits. However, reduction in  $V_{dd}$  leads to an increase in delay, which results in performance degradation of the circuit. Scaling down the threshold voltage,  $V_{th}$  by the same factor as  $V_{dd}$  is considered to be a solution to keep the same performance level. Unfortunately, reducing  $V_{th}$  in smaller geometry MOSFETs results in an exponential increase in the static power. The main component of the static power is the subthreshold leakage current. In order to solve this problem, multi-threshold CMOS was recommended to control leakage power. For large scaled integration (LSI) circuits, multithreshold voltage CMOS

(MTCMOS) circuit technology was proposed by inserting high-threshold devices in series to normal circuitry [3], [4]. However, only the standby leakage power can be reduced and the large inserted MOSFET's will increase the area and delay. Moreover, the data retention must also be considered.

Due to exponential dependence of leakage on threshold voltage ( $V_{th}$ ), a number of approaches have been developed using  $V_{th}$  as the key parameter to control leakage power dissipation. The leakage reduction methodologies can be classified into two broad categories depending on whether it reduces standby (static mode) leakage or runtime (active mode) leakage. For all the related researches, there are three main approaches to reduce standby leakage: input vector control (IVC), body bias control (BBC), and utilizing the MTCMOS technology. Several well-known static approaches for runtime leakage reduction applied at design time are dual- $V_{th}$  assignment [5], dual- $V_{th}$  assignment with transistor sizing [6]. In this paper we have implemented dual-  $V_{th}$  assignment approach to a 32-bit ripple carry adder using different threshold voltages. The results are compared with three different topologies of full adder namely, CMOS logic style, transmission gate logic style and pseudo-nmos logic style.

## 2. STATIC POWER ESTIMATION

The leakage power of a CMOS circuit is determined by the leakage current through each transistor, which has two main sources: reversed-biased diode-junction leakage current and subthreshold leakage current. Diode-junction leakage is very small and can be ignored [1]. Subthreshold leakage exponentially increases with the reduction of threshold voltage, making it critical for low-voltage circuit design. Therefore, in simulation, the focus is on subthreshold leakage power estimation.

The general method of computing leakage power for a large circuit involves the following steps. Given a particular set of circuit input values, determine which pull-up and PDN's are turned off. Within each network, the transistors which are turned on can be treated as short circuits. Transistors that are parallel to a transistor that is turned on can be eliminated from the leakage calculation.

Assuming the BSIM2 model [8], the subthreshold current of a MOS transistor is approximated as:

$$I_{Sub} = A e^{\frac{q}{nKT}(V_G - V_S - V_{th0} - \delta V_S + \eta V_{DS})} (1 - e^{-\frac{qV_{DS}}{KT}}) \quad (1)$$

where, n = subthreshold swing coefficient of the transistor

$V_{th0}$  = zero bias threshold voltage

$\delta$  = body effect coefficient

$\eta$ = drain induced barrier lowering (DIBL) coefficient.

$$A = \mu_0 C_{ox} \frac{W}{L_{eff}} \left(\frac{KT}{q}\right)^2 e^{1.8} \quad (2)$$

here,  $\mu_0$ = zero bias mobility,

$C_{ox}$  = gate oxide capacitance per unit area.

The standby leakage power of a logic circuit can be expressed as follows:

$$P_{stdby} = (\sum_i I_{stdby}) \cdot V_{dd} \quad (3)$$

where,  $I_{stdby}$ = standby leakage current through each node  $i$ .

It may be noted that  $I_{stdby}$  depends on the gate topology as well as the input signal levels. The leakage current, in fact, refers to the current that flows after all charge stored in “isolated” internal nodes has been discharged and therefore the magnitude of this current can be determined completely by the input signal levels. An internal node is isolated if there is no path either to  $V_{dd}$  or GND.

If transistors are connected in parallel and are both turned off (such as in the pull-down network of an NOR gate), then the values of  $\eta$  and  $A$  are the same for each transistor. The leakage contribution of each transistor can be calculated separately and added together. However, things become more complicated if they are in series.

Subthreshold leakage current strongly depends on  $\eta$  and temperature. If the internal-node capacitance is small and temperature is high, the given method can also be used to estimate active leakage power of low- circuits, especially at low-switching activities. Considering the fact that standby leakage current depends on input signal levels, the average leakage power can be evaluated with random patterns applied to primary inputs.

### 3. ADDER TOPOLOGIES

The implementation of the dual threshold voltage technique in a 32-bit ripple carry adder using different logic styles. In general ripple carry adders are used among all types of adders for its compact design and accuracy, but is the slowest of them all.

An N-bit adder can be constructed by cascading N full adder (FA) in series, connecting  $C_{o,k-1}$  to  $C_{i,k}$  for  $k=1$  to  $N-1$ , and the first carry-in  $C_{i,0}$  to 0. This configuration is called a ripple carry adder, since the carry ripples from one stage to the other. The full adder can be implemented from any one of the existing topologies. In this paper three topologies used for implementing the full adder: CMOS logic style, transmission gate logic style and pseudo-NMOS logic style

Conventional CMOS full adder [1],[2],[9], as shown in Fig. 1, is the complementary CMOS structure, which combines transistor PMOS pull-up and transistor NMOS pull-down network to produce output. The complementary CMOS logic circuit has the advantage of stability at low voltage. It has a high transistor count which consumes area and power. The problem of this adder is delay imbalance. Because the sum signal relies on the generation of carry-out signal, there is a delay between two signals. In this paper a mirror adder design using 28 transistors is implemented which is an improved adder design. In this

design the pull-up and the pull-down networks of the gate are dual and the NMOS and PMOS chains are completely symmetrical, which yields correct operation due to self-duality of both sum and carry functions. The transistors are optimized for speed. The resulting transistor sizes are annotated on Fig 2 where a PMOS/NMOS ratio of 2 is assumed.

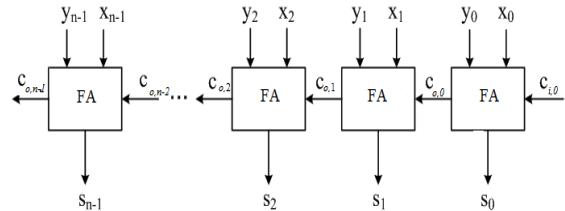


Figure 1. N-bit ripple carry adder

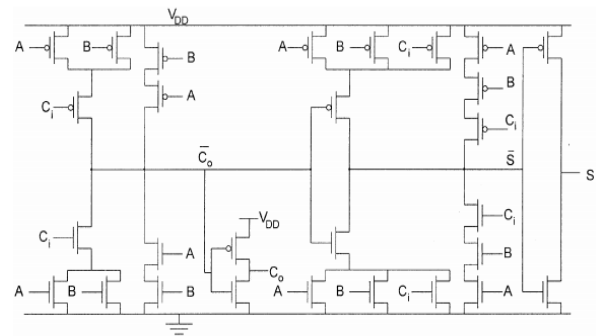


Figure 2. Static CMOS Mirror adder

The transmission gate full adder is illustrated in Fig. 3, which based on transmission gate and uses 24 transistors. It has lower-transistor count than CMOS style and lower loading of the input. It provides transistor buffer output of sum and carry for a high driving capability and has similar delays for sum and carry outputs

In pseudo-NMOS logic[1], which is a ratioed logic the entire pull-up network is replaced with a single unconditional load device that pulls up the output for a high output as shown in Fig.4. Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull-down network that realizes the logic function, and a simple load device. The clear advantage of pseudo-NMOS is the reduced number of transistors ( $N+1$  versus  $2N$  for complementary CMOS).

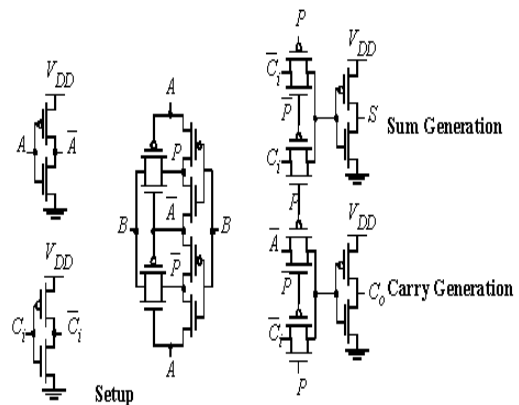


Figure 3. Transmission-gate-based full-adder cell with sum and carry delays of similar value[1]

The nominal high output voltage ( $V_{OH}$ ) for this gate is  $V_{dd}$  since the pull-down devices are turned off when the output is pulled high (assuming that  $V_{OL}$  is below  $V_{tn}$ ). On the other hand, the nominal low output voltage is not 0 V since there is a fight between the devices in the pull-down network and the grounded PMOS load device. This results in reduced noise margins and more importantly static power dissipation. The sizing of the load device relative to the pull-down devices can be used to trade-off parameters such a noise margin, propagation delay and power dissipation. A major disadvantage of the pseudo-NMOS gate is the static power that is dissipated when the output is low through the direct current path that exists between  $V_{DD}$  and GND.

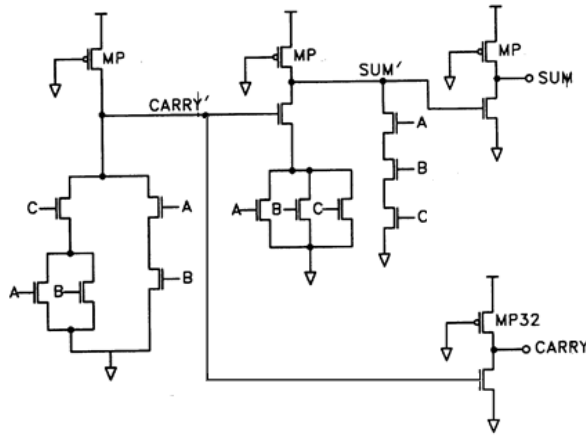


Figure 4. Pseudo-NMOS based full adder

#### 4. DUAL THRESHOLD ASSIGNMENT ALGORITHM

The basic approach is to use two different threshold voltages ( $0.2V_{dd} \leq V_{th} \leq 0.5V_{dd}$ ) in the same circuit [10]. For a logic circuit, the critical path (path with the longest propagation delay) is identified. A higher threshold voltage can be assigned to some transistors in noncritical paths so as to reduce leakage current, while the performance is maintained due to the low-threshold transistors in the critical path(s). Therefore, no additional transistors are required, and both high performance and low power can be achieved simultaneously.

The first step in our algorithm is to initialize a circuit with a single low threshold voltage. The next step is to assign a high threshold voltage to some transistors on noncritical

paths. Assign transistors to high threshold such that critical path delay does not degrade. Optimize the circuit in order to minimize the leakage power. In a ripple carry adder the carry path is the longest path and hence we assign low  $V_{th}$  transistors to carry path and high  $V_{th}$  transistors to other paths.

Dual threshold technique is good for leakage power reduction during both standby and active modes. Dual-threshold voltages can be achieved by body biasing [11]. A source to well reverse bias can be applied to some transistors to achieve high thresholds.

However, due to the complexity of a circuit, not all the transistors in noncritical paths can be assigned a high-threshold voltage; otherwise, the critical path may change, thereby increasing the critical delay. Whether a node can be assigned a higher depends on the value of the high threshold. If it is too small, there is little difference of propagation delay between low- and high transistors.

Hence, more nodes can be assigned high without influencing the critical delay, but the leakage current improvement for each high- transistor would be small. On the other hand, if the high-threshold voltage is too large, the leakage current can be reduced by a large amount for each such transistor. However, fewer nodes can be modified. Hence, among the allowable values for high-threshold voltage, there exists an optimal one.

#### 5. RESULTS

The method to reduce leakage power using dual threshold transistors has been implemented in Cadence Virtuoso Schematic editor using 90nm technology in a 32-bit ripple carry adder. The layout is designed using Cadence Virtuoso Layout suite. The intention is to optimize both power and delay of the circuit, the power-delay product (PDP), that is, the energy consumption has been minimized in the dual threshold assignment approach. The circuits were simulated at 1V supply voltage. All the transistors were initially set to a low threshold voltage of 0.2V and using BFS (Breadth-first-search) approach the transistors on non-critical paths were assigned high threshold voltage. A high threshold voltage is applied on non-critical paths and their results are tabulated as shown in Table 1. The results are compared with that of the circuit having a single threshold voltage.

The leakage power constitutes 51% of the total power in case of CMOS circuits in the original circuit with single- $V_{th}$ . This is reduced to more than 50% using dual threshold technique.

TABLE I. Simulation Results in 32-Bit Ripple Carry Adder with Dual Threshold Voltage Assignment and their Comparison with Single  $V_{TH}$

Adder style	Conventional Circuit				Circuit with dual threshold voltage					
	$V_{in}=0.2V$				$V_{in(crit)}=0.2V$ $V_{in(non-crit)}=0.448V$					
	Power (mW)	Delay (ns)	Leakage ( $\mu W$ )	PDP (pJ)	Power (mW)	Delay (ns)	Leakage ( $\mu W$ )	PDP (pJ)	Delay (% increase Over Low Vt)	Leakage reduction factor over low Vt
CMOS	0.790	0.846	2.15	0.6681	0.363	0.879	1.8	0.319	0.03(3.9% increase)	0.35(16.3% decrease)
TG	0.540	1.72	4.8	0.9288	0.268	2.14	1.5	0.572	0.42(24.4% increase)	3.3(68.75% decrease)
Pseudo-NMOS	2.80	0.502	2130	1.41	2.69	0.580	1650	1.56	0.07(15.5% increase)	480(22.54% decrease)

Comparison of power, delay, power delay product and leakage for 32-bit adder is shown figures below for CMOS, Transmission gate and Pseudo NMOS logic families with single  $V_t$  and dual  $V_t$ . The red colour is for dual  $V_t$  and blue colour is for single  $V_t$  implementation.

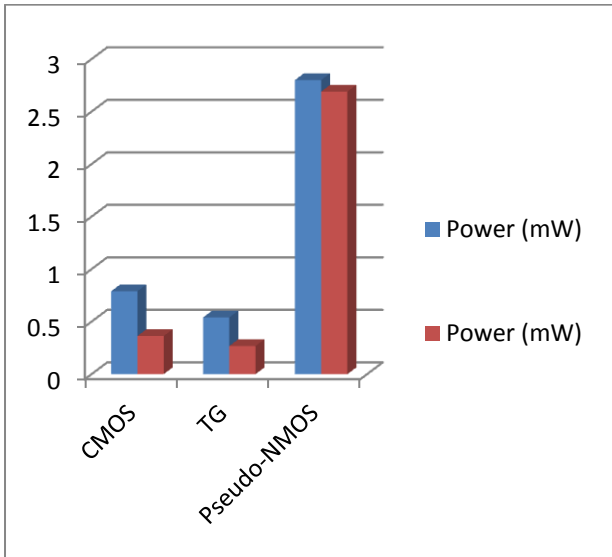


Figure 5.1 Comparison of power for single  $V_t$  and Dual  $V_t$  in CMOS, TG and Pseudo-NMOS

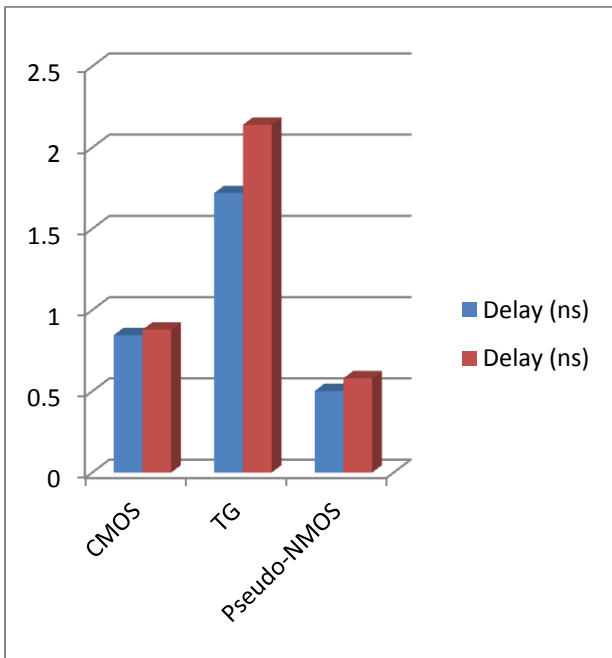


Figure 5.2 Comparison of delay for single  $V_t$  and Dual  $V_t$  in CMOS, TG and Pseudo-NMOS

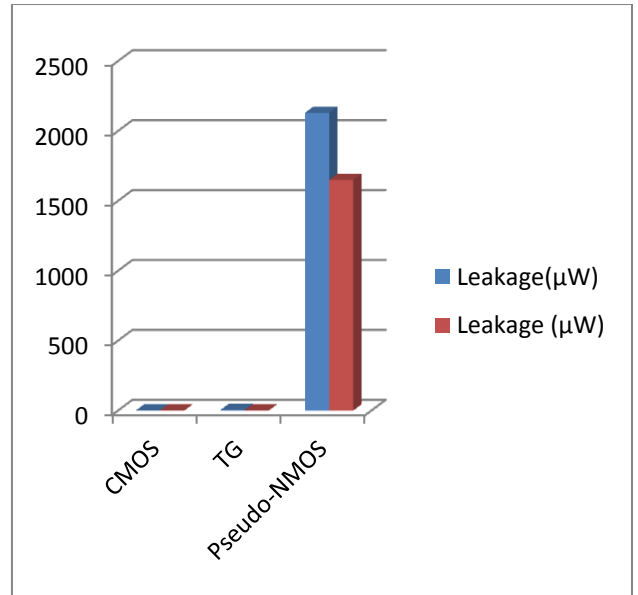


Figure 5.2 Comparison of delay for single  $V_t$  and  $V_t$  in CMOS, TG and Pseudo-NMOS

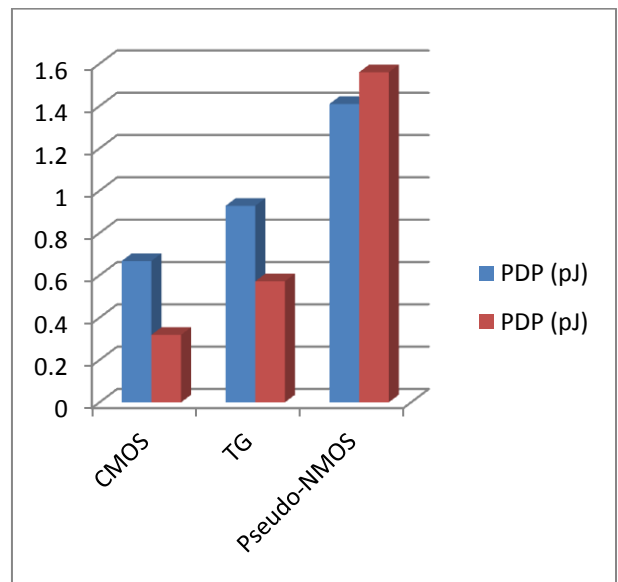


Figure 5.2 Comparison of power delay product for single  $V_t$  and  $V_t$  in CMOS, TG and Pseudo-NMOS

The layout of 1-bit full adder with dual threshold technique is given in Fig. 4(a), 4(b), 4(c)..

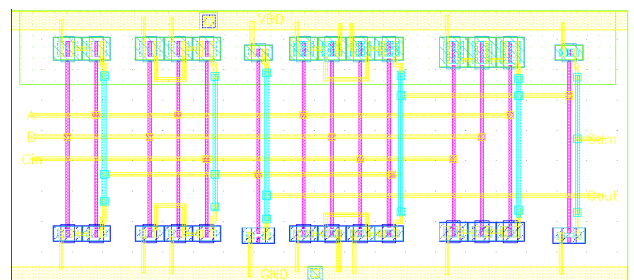


Figure 4(b) Layout of 1-bit full adder using CMOS logic implementation

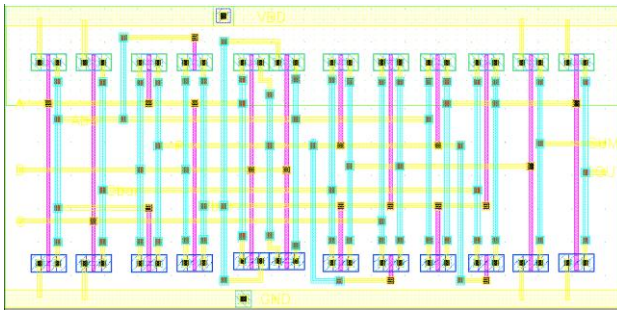


Figure 4(a) Layout of 1-bit full adder using transmission gate logic implementation

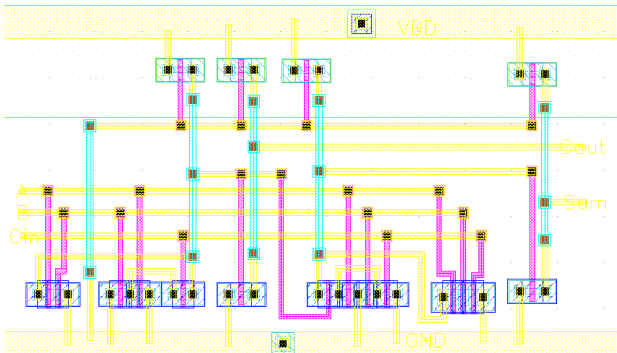


Figure 4(b) Layout of 1-bit full adder using Pseudo-NMOS logic implementation

## 6. CONCLUSION

In this paper, a low power 32-bit ripple carry adder is designed using dual threshold voltage technique. The simulation was carried out using standard Cadence Virtuoso tools with 90-nm technology with a supply voltage of 1V. the layout of 32-bit ripple carry adder is further designed using Cadence Virtuoso layout and the parasitic values are extracted. The results show a reduction in leakage power and improvement in PDP (power delay product) using dual threshold technique as compared to single threshold voltage design.

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