A Comparative Study of Methodologies to Optimize Post- layout Challenges

Bhawana Jain
MANIT, Bhopal

Kavita Khare, PhD
Professor,
MANIT, Bhopal

ABSTRACT
Shrinking technology enables designers to integrate more functionality with improved performance and density in ICs; but this improvement comes at cost. The impacts of parasitic are dominating circuit performance with leading edge of technology. This paper first presents the post-layout challenges facing by the designers at advanced technology node and then discusses the different advanced techniques used to mitigate those challenges. We can bucket these post-layout challenges mainly in two categories; first "*PARASITC EXTRACTION* related challenges" and second "*POST-LAYOUT SIMULATION* related challenges" which includes accuracy, run time and memory usage uses issues. They are causing negative impact on product yield and time-to-market constraint. Finally we conclude this paper by comparing different-different methodologies used for parasitic extraction and simulation.

In summary, In this paper we will discuss the advanced techniques used for the Parasitic extraction and Simulation for the successful tape-out.

Keywords
Parasitic extraction, Post-layout Simulation, Interconnect Resistance, Interconnect Capacitance, Extracted netlist.

1. INTRODUCTION
Nanometer technology scaling to the leading edge nodes (28nm/14nm or below) demands higher accuracy and performance with good productivity. Deep sub threshold nanometer processes introduces multi-layer, closely-spaced, thin and tall metal interconnects which results in large number of interconnect resistances and capacitances (millions of new parasitic effect in design), hence circuit performance dominated by parasitic delays. In today's era designers strongly needs advanced technique which reduce the gap between the parasitic values estimated during implementation and results of post-layout extraction. Parasitic needs to extracted and simulated with sufficient accuracy to enable design team to, at least, find and fix violations like setup, hold and glitches confidently. The sensitivity of the parasitic to the process variation also need to understood well enough to avoid the yield loss.

IC designer need an advanced parasitic extraction solution to boost simulation performance and designer productivity.

The rest of this paper is organized as follows. The challenges facing by the designer during parasitic extraction and post-layout simulation is explained in section 2. The basic post-layout design flow is discussed in section 3. Section 4 covers the advanced extraction techniques and section 5 covers the advanced simulation techniques. Finally paper concluded in section 6 followed by acknowledgment and references.

2. POST-LAYOUT CHALLENGES
Shrinking technology provides great benefits. The benefits, however come with a small but negotiated cost. We have classified post-layout challenges in two categories. They are as follows:

2.1 Parasitic Extraction related challenges
Moore's law is the empirical observation that component density and performance of integrated circuits every year, which then revised to doubling every two years [8]. As the space between transistors becoming too small parasitic become real limiters. Figure 1 shows various parasitic resistances and capacitance related to planar MOSFET, Which were ignored for previous technology nodes. From figure 1 it is clear that source/drain contact and gate are only tens of nano meters apart, which results in higher contact resistance and gate-to-contact capacitance. The intrinsic channel resistance and capacitance being proportional to gate length have reduced dramatically during past four decades. Because of such dramatically reduction in channel resistance, parasitic resistance and capacitance are now becoming comparable and are on the verge of becoming even larger than the intrinsic device resistance and capacitances.

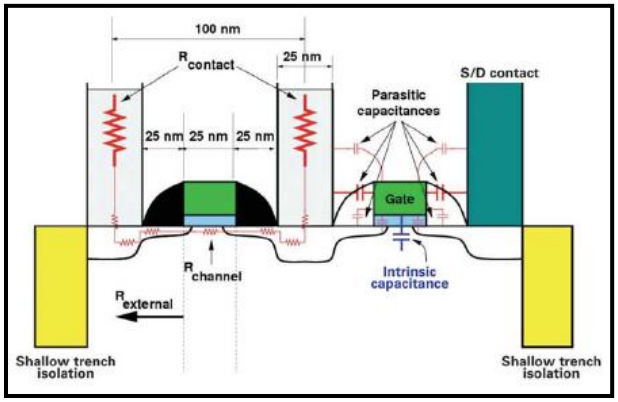

Fig 1: Planer CMOS Schematic Showing Various Parasitic Resistances and Capacitances [8]

As the number of transistors increases, the number of nets also increases proportionally. This means that extraction tool has to extract, manage and pass much amount of data to the simulator. In the earlier nodes only capacitors were extracted but now a day's resistance plays an important role. Since resistance is a function of temperature, extraction process needs to be run multiple times for multiple temperatures. With advanced technology number of process corners is also increased. Designers are facing problems due to large extraction run time and unmanageable volume of data (billions of transistors and millions of parasitic).

2.2 Post-Layout Simulation Related Challenges

Simulation challenges creates larger bottleneck in post-layout verification as compared to parasitic extraction. Simulation run time and capacity are directly related to the parasitic netlist size and the number of parasitic elements or nodes in the generated netlist. Parasitic extraction of full-chip with all the nets results in huge netlist size and can lead to unnecessary simulation inefficiency with same accuracy (not improved accuracy). As designers moved from "C" to "RC" post-layout verification, the extracted netlist to be managed and simulated has blown up and it directly cost to simulation run time. Another major challenge is a need of varying simulation process corners (voltage, temperature e.t.c.), due to the designer's specific application need. Designers need to rerun simulation process multiple time for multiple process corners which is heavy loss in simulation run time and disk usage. But the comprehensive post-layout simulation are required to capture the nanometer effect in order to reduce the risk that a design passes verification before tape out, but fails after fabrication.

3. BASIC PRE AND POST LAYOUT DESIGN FLOW

Figure 2 sowing the typical pre-layout and post-layout design flow. Once the schematic and layout of design is completed designers apply various checks like layout vs schematic check and design rule check. Then parasitic extraction should be perform to analyze actual circuit performance. The reason behind the parasitic extraction is to create an accurate analog model of the circuit, so that detailed simulation can give actual circuit responses and the pre – layout simulation result does not contain the effect of parasitic.

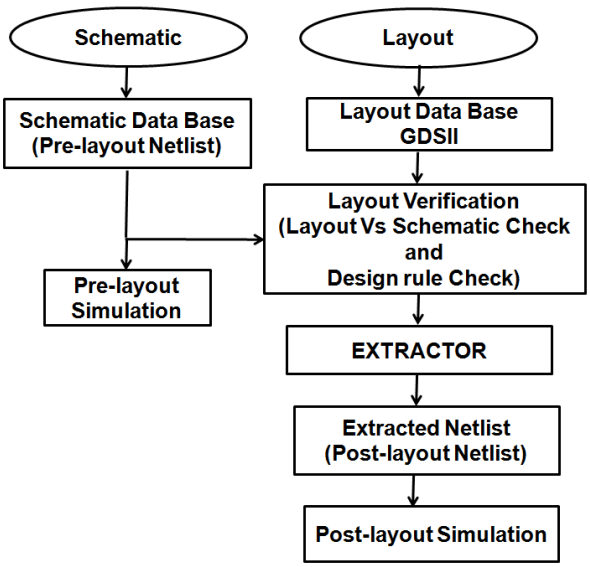

Fig 2: Design Flow

We can classify simulators in two categories first is traditional true spice simulators which build a single matrix to solve the circuit, are suitable for accuracy, but they are too slow to simulate an entire circuit and second is accelerated fast spice simulator which are smart enough to apply partition algorithm, and support for various type of models ranging from complex to simple device models so that it is flexible to configure, depending on the accuracy needed with optimized simulation run time[5]. Since the netlist are becoming bigger and complex use of traditional simulators are very tedious job. Fast-spice simulators use matrix portioning, model simplification, RC reduction techniques to accelerate simulation and expand capacity beyond that of traditional spice simulators. The need for fast-spice simulator is arises because the design sizes exceeding the capacity limit of traditional spice simulators and need to simulate nanometer effects using large post-layout parasitic RCs. In this paper we present the useful techniques provided by fast-spice simulators to address the outlined challenges [2].

To analyze the impact of parasitic on the simulator run time, we have run the simulation using fast spice simulator on a memory design and seen that if the pre-layout simulation takes X time then post – layout simulation takes 2.5X for capacitive netlist and 4.5X for "RC" netlist.

4. ADVANCED EXTRACTION AND SIMULATIO N TECHNIQUES

To address all the outlined challenges many techniques have been developed. In this paper we will discuss all the advanced techniques for parasitic extraction and post-layout simulation.

4.1 Hierarchical Extraction and Simulation

This methodology offers IC designers a great option to improve design's post-layout verification and this techniques supported by many extraction tools (for example starRC from Synopsys, Calibre from Mentor graphics). Since flat extraction allows all coupling effects to be taken into consideration, the runtime can be too long and file size of extracted netlist should be very large. Flat parasitic extraction all though a most accurate method but it is very time consuming for big design circuits. Hierarchical extraction can be use to tackle these challenges. In hierarchical extraction, each level of hierarchy is extracted separately and then each level of parasitic is stitched together. The upper levels of hierarchy can see coupling capacitance effects into lower levels of hierarchy, but then the coupling is grounded. This is known as a "grey box flow"[2].

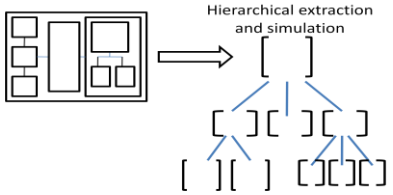

Fig 3: Hierarchical Extraction and Simulation

The hierarchical extraction technique allows designers to do "bottom-up" or "top-down" simulation. Figure 3 showing the hierarchical extraction which improves the run time by extracting the entire block hieratically. Following are the points which will describe the flat vs hierarchical extraction technique:

1) Improves the run time to downstream the netlist to simulation tool. The addition of hierarchy makes the netlist small comparatively.

2) With flat extraction it is difficult to debug errors in verification, as millions of errors in the flattened netlist may be due to an error in one block in the hierarchy [11].

4.2 Selected Net Extraction

In this technique user can extract particular net from the overall design for performing specific analysis such timing analysis etc. In this method the user can specify the path and name of the parasitic resistor netlist. By setting a coupling threshold, the tool will express net to net capacitance only if the capacitance value is above the threshold. All of the capacitance value that are lower than the threshold will be replaced with ground capacitance of the same value. When replacing the coupling capacitance between two nets a corresponding ground capacitance is added to both nets involved. The RC parasitic extractor tools allows user to perform parasitic extraction on a specified list of nets or the user can select to ignore some nets. This will help user to reduce the size of post-layout netlist file and accelerate the simulation run time. User can only select the net which highly impact the circuit performance and can do extraction for that net only [7].

4.3 RC Reduction to Accelerate Simulation

The simulation runtime is proportional to the number of parasitic elements. The nodes or parasitic information which needs to be passed to post layout simulation tools are decided by circuit behavior and functional requirements. A technique of Selective filtering is done for the parasitics which may have less significance over circuit performance. This technique is called as RC reduction. Small values of resistive and capacitive elements have significant effect on the runtime. Due to this reason, their effect is nullified by replacing them suitably with short circuits or open circuits with the help of appropriate simulator option. These small values of resistance and capacitance have no effect on the response of the system hence nullifying its effect does not impact the circuit accuracy [6].

This technique offer major advantages in terms of control in the netlist size and enhancement in the simulation runtime performance with no loss in accuracy.

4.4 Parasitic Back-annotation for Simulation

The two file which are needed for the back-annotation simulation are the first one is schematic netlist which is also known as pre-layout netlist and the second is parasitic extracted netlist [6]. Since DSPF/SPICE file is very large and the extracted parasitic of each net does not impact the timing performance, considering full DSPF will be an overhead on simulation runtime and resources. With this feature, we can smartly tell the simulator to consider only the specified nets; it is known as DSPF back-annotation. Different-different simulators have different commands for the back-annotation flow. Back annotation process is simply back-annotate the schematic netlist net name to the layout extracted netlist. Hierarchical back-annotation enables designers of large memory and custom ICs to achieve the best combination of fastest simulation turn-around time and golden signoff accuracy. In this technique user can reuse the pre-layout simulation stimuli based on the schematic netlist based on their post-layout simulation with the extracted parasitic netlist [7]. This methodology allows designers to easily annotate the post-layout parasitic onto the pre-layout schematic netlist. Figure 4 showing the parasitic back annotation to the schematic netlist.

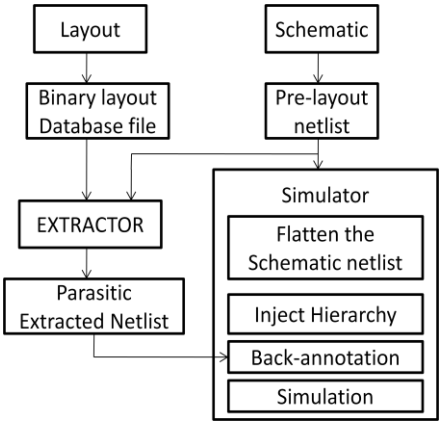

Fig 4: Back-annotation flow

4.5 Simultaneous Multi Corner Extraction

This feature of extraction is provided by StarRC extraction tool which is from synopsys. Since we have already discussed that with the scaling in technology, number of process corners is increasing and for designer it is very difficult to manage those file. Hence to address those challenges designer can use this technique. In this technique user can extract parasitic for multiple temperature and multiple process corners parallelly and analyzed in single go. There is no need to do setup and then run extraction multiple time for multiple corners. Hence this technique minimizes the designer's effort and also tremendous improvement in extraction run time and significantly reduces the disk usage. With this methodology run time speed-up of 3X is achieved when we compare it with traditional methodology of extraction [13]

5. CONCLUSION

SoC circuits are designed using billions of transistors. To prevent design from the failure due to sub-nanometer effect, proper analysis of circuit should be required. Memory, standard cell, analog/mixed-signal IC etc designer's need efficient tools and methodology for post-layout extraction and simulation to address the problems of accuracy, large run time and huge disk usage caused by increasing design sizes, growing count of parasitic, dominating effect of parasitic in design, new process corners to effectively meet their design and project schedule challenges. In this paper we have done the comparative study of multiple technique of extraction and simulation tool to boost post-layout simulation performance and capacity with preserving signoff accuracy.

6. ACKNOWLEDGMENTS

The authors would like to thank Dr. Appu Kuttan K. K., Director MANIT Bhopal and Dr. Ajay Somkuwar, Professor and HOD Electronics & Communication Engineering Department MANIT, Bhopal for providing all the necessary facilities for the research.

7. REFERENCES

[1] Eileen You, Swee Yav Choe, Chin Kim, Lakshminarasimh Varadadesikan, Kathilgamar Aingaran, John MacDonal, "Parasitic Extraction for Multimillion-Transistor Integrated Circuits: Methodology and Design Experience", IEEE 2000 Custom Integrated Circuits Conference.

[2] Sundaram Sangameswaran and Sho Yamauchi, "Post-Layout Parasitic Verification Methodology For Mixed-Signal Designs Using Fast-Spice Simulators", IEEE 2005.

[3] Karen Chow, "The Challenges and Impact of Parasitic Extraction at 65 nm", Proceedings of the 7th International Symposium on Quality Electronic Design (ISQED'06).

[4] Weibing Gong, Wenjian Yu, Yongqiang Lu, Qiming Tang, Qiang Zhou, Yici Cai, "A Parasitic Extraction Method of VLSI Interconnects for Pre-Route Timing Analysis", IEEE2010.

[5] Michał Rewienski, "A Perspective on Fast-SPICE simulation Technology" Springer Science+Business Media B.V. 2011.

[6] Application Note on "Parasitic Back Annotation for Post Layout Simulation"

[7] Omar Shah and Shekhar Kapoor, "Extraction Techniques for High-performance, High-capacity Simulation", Synopsys white paper 2009

[8] Scott E. Thompson and Srivatsan Parthasarathy, "Moore's law: the future of Si microelectronics", Materials today volume 9, 2006.

[9] William H. Kao, Chi- Yuan Lo, Mark Basel and Raminderpal Singh, "Parasitic Extraction: Current State of the Art and Future Trends", PROCEEDINGS OF THE IEEE, VOL. 89, NO. 5, MAY 2001.

[10] Paul-Franzon and Mark S. Basel, " Panel: Parasitic extraction accuracy; How much is enough?",

[11] Saisanthosh Balakrishnan and Charlie C.P. Chen, "SeaPEEC: A Comprehensive Hierarchical Parasitic Extraction Tool Based on Partial Element Equivalent Circuits".

[12] "Parasitic Extraction of FinFET-based Memory Cells ", http://www.silvaco.com/content/appNotes/iccad/2-005_Guardian.pdf

[13] Datasheet of "StarRC; Parasitic Extraction", Synopsys