DTMOS Transistor with Self-Cascode Subcircuit for Achieving High Bandwidth in Analog Applications

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ABSTRACT
In this work, an improved dynamic threshold MOS (DTMOS) transistor with self-cascode subcircuit has been proposed in this work. By adopting the self-cascode subcircuit, the proposed DTMOS transistor could be operated at supply voltage over 0.7V. Apart from this, simulation results for the proposed DTMOS, also demonstrate improvement in the transconductance and bandwidth by a factor of 2.31 and 1.59 respectively. Furthermore, the current driving capability of proposed DTMOS transistor has increased by a factor of 1.87. To validate the proposed concept and its applications in analog circuits, a current mirror and a differential amplifier have been designed in 180nm CMOS technology. Both circuits are able to operate at higher bandwidth as compared to their conventional counterparts. The Monte Carlo simulations reflect the robustness of the circuits to device mismatch errors. The proposed DTMOS transistor is more suitable for large signal circuits such as mixer and voltage control oscillator.

Keywords
Dynamic threshold MOS transistor (DTMOS), Self-Cascode, bandwidth, transconductance, analog integrated circuits.

1. INTRODUCTION
The need for analog circuits in modern mixed-signal VLSI chips for multimedia, perception, control, instrumentation, medical electronics and telecommunication is very high. The continuous trend towards smaller feature size for transistors in the CMOS technology demands for lower supply voltages [1]. But the value of the MOS threshold voltage (V_{th}) doesn't proportionally decrease with device size reduction, which poses a great challenge to CMOS analog circuit design. Lowering the power supply voltage often sacrifices the speed, noise requirements, dynamic range, gain, bandwidth and linearity in analog circuit. This trend has forced most analogue basic building blocks to be redesigned, in an attempt to guarantee their overall same performance or better than their operation for larger power supplies. This requires traditional circuit solutions to be replaced by new circuit design techniques [2].

The shrinking sizes of semiconductor devices in CMOS technology entail the simultaneous reduction of supply voltage and threshold voltage of MOS transistor. Since the threshold voltage of MOS transistor is not reduced at the same rate as the power supply, it becomes increasingly difficult to design wideband analog circuits because of the reduced voltage headroom. Analog signal processing circuits now operating from single 1.5V supplies and dropping, are constantly demanding higher bandwidth and speed performances. To overcome the issue of threshold voltage scaling limitation, dynamic threshold MOS transistor was proposed by Assederaghi et al. in their pioneering papers [3,4] for silicon on insulator (SOI) process technology. Since the first introduction of DTMOS in 1994, many novel and interesting proposals have been made regarding this transistor.

The main limitation of DTMOS transistor is that the gate input has to be limited to approximately one diode voltage otherwise large body-source/drain junction capacitances and currents will result. Few proposals have been made to eliminate this low-voltage operation limit [5-7]. These ideas revolve around using auxiliary MOSFETs or diodes to clamp the body-source forward bias value with the penalty of increased capacitive loading and layout area. In this work, it has been proposed to eliminate this low-voltage operation limit using self-cascode subcircuit which is inserted between the gate and body terminals of conventional DTMOS transistor. This configuration prevents direct connection between the gate and body terminals and as a result, the proposed DTMOS transistor can operate above 0.7 V. and obtains a higher current drive, transconductance and bandwidth as compared to conventional DTMOS transistor.

The paper is organized as follows. In section 2, the principle of conventional DTMOS transistor is presented and its main features are emphasized with the help of its small signal model. In section 3, the proposed DTMOS with self-cascode as a sub-circuit and its small signal analysis is presented. Simulation results for the proposed DTMOS transistor are presented in section 4. Applications of the proposed DTMOS in the design of a current mirror and differential amplifier is given in section 5. Conclusions are summarized in section 6.

2. CONVENTIONAL DTMOS TRANSISTOR
For low voltage low power design, various techniques have been reported so far in literature. The main focus of all the techniques have been to overcome the difficulties introduced by the relatively high threshold voltage of MOS transistor. Bulk driven is one of those techniques, where input signal is applied at body terminal instead of gate terminal, after biasing the gate terminal to a sufficient voltage. Thus the threshold voltage drop is removed from signal path [8]. Unfortunately, the transconductance of a bulk driven MOS transistor is substantially smaller and the equivalent input referred noise is higher than that of a conventional gate driven MOS transistor, which may result in lower gain bandwidth and worse frequency response[9]. The basic DTMOS structure proposes to use both the gate and the body terminal to provide the signal input. This approach, shown in and first presented in [3], preserves some of the advantages of gate driven MOS transistor and overcomes some of the limitations of bulk driven MOS transistor.

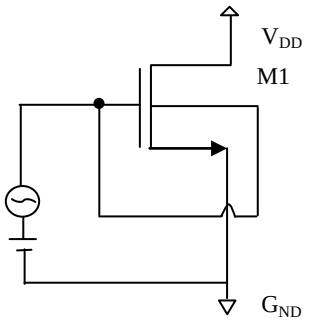

Fig 1: Conventional DTMOS transistor

Due to dynamic body bias voltage, the threshold voltage (V_T) of MOS transistor becomes function of input signal. With applied input signal at gate terminal, bias voltage at body terminal changes dynamically as input changes. Thus, V_{GS}=V_{BS} is maintained all the time as gate and body terminals are shorted together. Here source-body junction gets slightly forward biased when gate input increases and V_T decreases due to the body effect [10]. Due to dynamic body bias, potential in the channel region is strongly controlled by the gate and body terminals, leading to a high transconductance owing to faster current transport. The relation between input signal and V_T is described using the following equation [11].

$$V_{T0} = 2\phi_B + V_{FB} + \frac{\sqrt{2q\varepsilon_s N_a(2\phi_B)}}{C_{ox}} \quad (1)$$

Where $V_{FB}$is the flat band voltage and $2\phi_B$ is the inversion layer voltage the inversion layer potential, $N_a$is the channel doping, $\varepsilon_s$is the Si permittivity, q is the electron charge. Considering body biasing, V_T is as explained in [9] is given as

$$V_T = V_{T0} + \gamma\left(\sqrt{\Psi_S + V_{BS}} - \sqrt{\Psi_S}\right) \quad (2)$$

where $\gamma = \frac{\sqrt{2q\varepsilon_s N_a}}{C_{ox}}$ and V_T is threshold voltage due to body effect i.e. applied V_{SB}, V_{T0} is the threshold voltage when V_{SB} is zero and mainly depends on the manufacturing process. γ is typically equals to 0.4V-0.5V and depends on the gate oxide capacitance, silicon permittivity, doping level and other parameters. ψ_s is surface potential in strong inversion and typically is 0.6V. ψ_s is assumed to | $2\Phi_F$ |, where Φ_F is Fermi potential.

The small signal model of conventional DTMOS transistor is shown in Fig.2. It has two transconductances, the gate transconductance (g_m)and body transconductance (g_{mb})[12]. And the relation between both the transconductance is given by

$$\frac{g_m}{g_{mb}} = \frac{C_{BC}}{C_{GC}} = 0.2 - 0.4 \quad (3)$$

where C_{BC}, C_{GC} are the total body-channel capacitance, the total gate channel capacitance. From Fig.2, the effective input capacitance is given as

$$C_{BC} \approx C_{gs1} + C_{bs1} \quad (4)$$

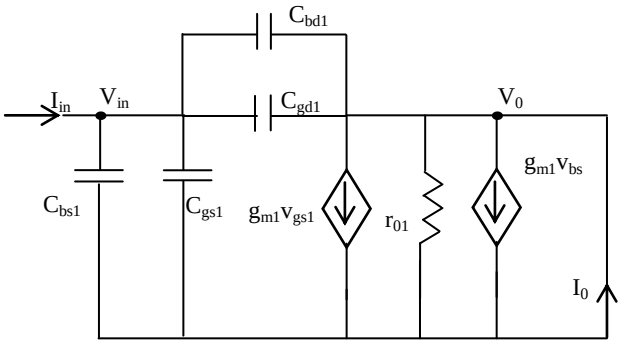

Fig 2: Small signal model of the conventional DTMOS transistor

From small signal model

$$V_{gs1}=V_{bs1} = V_{in} \quad (5)$$

Applying KCL at the input node

$$I_i = V_{in}(sC_{bs1}+sC_{gs1}) + (V_{in} - V_O)(sC_{bd1}+sC_{gd1}) \quad (6)$$

Applying KCL at the output node

$$I_0 = \frac{V_O}{r_{01}} + g_{mb1}V_{gs1} + g_{m1}V_{gs1} + (V_{in} - V_O)(sC_{bd1}+sC_{gd1}) \quad (7)$$

Using value of V_{gs} from Eq.5 in Eq.7

$$I_0 = \frac{V_O}{r_{01}} + (g_{mb1}+ g_{m1})V_{in} + (V_{in} - V_O)(sC_{bd1}+sC_{gd1})$$

For finding f_t, Short circuit current gain = unity i.e., $I_0 (V_0 = 0) = I_i$. Putting $V_0 = 0$ in Eq.6 and Eq.7 and neglecting r_{01} ,

$$I_0 = I_i \quad (8)$$

$(g_{mb1}+ g_{m1}-sC_{bd1}-sC_{gd1}) = (sC_{bs1} + sC_{gs1} + sC_{bd1}+ sC_{gd1})$

$$\omega_t = \frac{(g_{m1}+g_{mb1})}{(2C_{gd1}+2C_{bd1}+C_{gs1}+C_{bs1})} \quad (9)$$

$$f_t = \frac{(g_{m1}+g_{mb1})}{2\pi(2C_{gd1}+2C_{bd1}+C_{gs1}+C_{bs1})} \quad (10)$$

Assuming $C_{gd1}=C_{gs1}=C_{gb1}=C_{db1}=C_{bs1} \approx C, g_{m1} = g_m$ and $g_{mb1} = g_{mb}$ in Eq.10, we get

$$f_t = \frac{(g_m+g_{mb})}{12\pi C} \quad (11)$$

It may be observed from Eq.11 that the transition frequency of a DTMOS transistor is varying linearly with the transconductance. Hence if the higher bandwidth is desired, then one of the possible solutions is to increase the transconductance of conventional DTMOS transistor.

3. PROPOSED DTMOS TRANSISTOR

The proposed DTMOS transistor with self-cascode subcircuit is shown in Fig.3. This subcircuit is a series connection of two conventional MOS transistors M2 and M3, which with an appropriate choice of sizes, work as a single long channel transistor with reduced output conductance. For m>1, the circuit behaves like a single long-channel transistor operating in saturation region but without severe channel length modulation effects. Effective size of DC equivalent long channel transistor is given as [13]

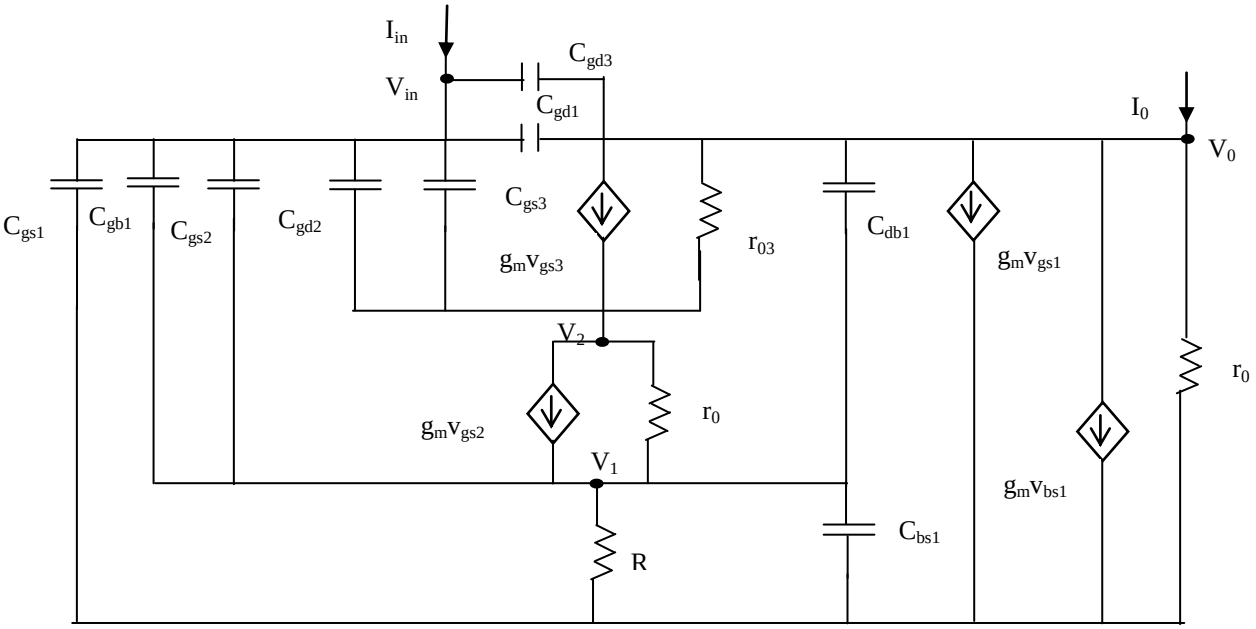

Fig.4 Small signal model of the proposed DTMOS transistor

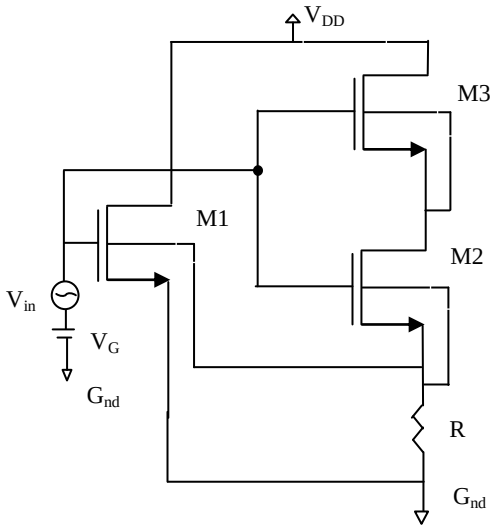

Fig 3: Proposed DTMOS transistor with self-cascode sub-circuit

$$\frac{W}{L}_{eq} = \frac{m}{m+1}\frac{W}{L} \quad (12)$$

where m is the quotient of the aspect ratios given as

$$m = \frac{W_2}{L_2}/\frac{W_3}{L_3} \quad (13)$$

The self-cascode subcircuit and a degeneration resistor R in the Fig. 3, is used to bias the body terminal of conventional DTMOS transistor M1. In order to supply identical voltages to both transistors, the drain terminals of M1 and M3 transistors are connected together, and the gate terminals of M3 and M2 transistors are also linked together. In conventional DTMOS transistor, gate and body terminals are shorted together whereas in the proposed DTMOS structure, high gain self-cascode subcircuit has been embedded between gate and body terminals of the conventional DTMOS transistor M1. This removes the 0.7 V limitation of conventional DTMOS transistor and at the same time increases the transconductance and bandwidth of the DTMOS circuit. By embedding the high gain self-cascode subcircuit in transistor M1, a large voltage difference between source and body terminals of transistor M1 has been generated and this increase V_{SB}. Due to the body effect threshold voltage of M1 decreases V_T and "ON" current increases. It is worth mentioning that proposed DTMOS structure has less parasitic capacitance as compared to the other structures proposed in the reported literature for removing the 0.7V limitation of conventional DTMOS circuit using diodes or inverters etc. For a fair comparison of the proposed DTMOS transistor with the conventional DTMOS transistor, both device sizes are kept identical, with the corresponding dimensions as listed. All the devices use the channel length of 180 nm and 260 nm diffusion width.

The small signal analysis of the proposed DTMOS with Self-Cascode sub-circuit is shown in Fig.4. From small signal model

$$V_{gs1}=V_{in} \quad (14)$$

$$V_{gs2}=V_{in}-V_1 \quad (15)$$

$$V_{gs3}=V_{in}-V_2 \quad (16)$$

$$V_{bs1}=V_1 \quad (17)$$

Applying KCL at input node,

$$I_i=V_{in}(sC_{gd1}+sC_{gd3}+sC_{gs3}+sC_{gd2}+sC_{gs2}+sC_{gb1}+sC_{gs1})-V_0(sC_{gd1}+sC_{gd3})-V_1(sC_{gs2}+sC_{gb1})-V_2(sC_{gs3}+sC_{gd2}) \quad (18)$$

Applying KCL at output node,

$$I_0 = g_{m1}V_{gs1}+g_{mb1}V_{bs1}+(V_O-V_1)sC_{db1}+g_{m3}V_{gs3}+(V_O-V_{in})sC_{gd3}+(V_O-V_{in})sC_{gd1}+\frac{V_O}{r_{01}}+\frac{(V_O-V_2)}{r_{03}} \quad (19)$$

Applying KCL at V_1 node

$$g_{m2}V_{gs2}=(V_1-V_0)sC_{db1}+V_1sC_{bs1}+(V_1-V_{in})\,sC_{gs2}+(V_1-V_{in})sC_{gb1}+\frac{(V_1-V_2)}{r_{02}}+\frac{V_1}{R} \quad (20)$$

Applying KCL at V_2 node,

$g_{m2}V_{gs2} + (V_2 - V_{in})sC_{gs3} + (V_2 - V_{in})sC_{gd2} = g_{m3}V_{gs3} + \frac{(V_O - V_2)}{r_{03}} + \frac{(V_1 - V_2)}{r_{02}}$ (21)

Now, Substituting $C_{gd1}=C_{gd2}=C_{gd3}=C_{gd}$, $C_{gs1}=C_{gs2}=C_{gs3}=C_{gs}$, $C_{gb1}=C_{gb}$. $C_{bs1}=C_{bs}$, $C_{db1}=C_{db}$, $r_{01}=r_{02}=r_{03}=r_0$, $g_{m1}=g_{m2}=g_{m3}=g_m$, $g_{mb1}=g_{mb}$ in Eq.19 and Eq.20, we get

$I_i=V_{in}(3sC_{gd}+3sC_{gs}+sC_{gb})-V_1(sC_{gs}+sC_{gb})-V_2(sC_{gs}+sC_{gd})-V_0(2sC_{gd})$ (22)

$I_0 = V_O(\frac{2}{r_0}+sC_{db}+2sC_{gd}) + V_{in}(2g_m-2sC_{gd}) + V_1(g_{mb}-sC_{db}) - V_2\left(\frac{1}{r_0}+g_m\right)$ (23)

$V_{in}(sC_{gs}+sC_{gb}+g_m) + V_0\, sC_{db} + \frac{V_2}{r_0} - V_1(sC_{db}+sC_{bs}+sC_{gs}+sC_{gb}+g_m+\frac{1}{R}) = 0$ (24)

$$V_1 = \frac{V_{in}(sC_{gs}+sC_{gb}+g_m)}{sC_{db}+sC_{bs}+sC_{gs}+sC_{gb}+g_m+\frac{1}{R}} \quad (25)$$

$$V_{in}(sC_{gs}+sC_{gd}) + g_mV_1 = V_2(sC_{gs}+sC_{gd}+g_m) \quad (26)$$

Substitute the value of V_1 from Eq.25 in Eq.26, we get

$$V_2 = \frac{V_{in}\left[(sC_{gs}+sC_{gd}) + \frac{g_mV_{in}(sC_{gs}+sC_{gb}+g_m)}{sC_{db}+sC_{bs}+sC_{gs}+sC_{gb}+g_m+\frac{1}{R}}\right]}{(sC_{gs}+sC_{gd}+g_m)} \quad (27)$$

To find f_t, Short circuit current gain= unity i.e., $I_0\,(V_0 = 0) = I_i$. Putting $V_0 = 0$ and neglecting r_0 in Eq.22 and Eq.23

$$I_0 = I_iV_{in}(5sC_{gd}+3sC_{gs}+sC_{gb}-2g_m) + V_1(-sC_{gs}-sC_{gb}+sC_{db}-g_{mb}) = V_2(sC_{gs}+sC_{gd}-g_m) \quad (28)$$

Now putting values of V_1 and V_2 from Eq.26 and Eq.27 respectively in Eq.28 and on solving we get

$$V_{in}(5sC_{gd}+3sC_{gs}+sC_{gb}-2g_m) + \frac{V_{in}(sC_{gs}+sC_{gb}+g_m)}{sC_{db}+sC_{bs}+sC_{gs}+sC_{gb}+g_m+\frac{1}{R}}(-sC_{gs}-sC_{gb}+sC_{db}-g_{mb}) = (sC_{gs}+sC_{gd}-g_m)\frac{V_{in}\left[(sC_{gs}+sC_{gd}) + \frac{g_mV_{in}(sC_{gs}+sC_{gb}+g_m)}{sC_{db}+sC_{bs}+sC_{gs}+sC_{gb}+g_m+\frac{1}{R}}\right]}{(sC_{gs}+sC_{gd}+g_m)} \quad (29)$$

On solving further and neglecting higher order terms, we get

$$g_m{}^3 + g_{mb}g_m{}^2 + 2\frac{g_m{}^2}{R} = s\,(\frac{4g_mC_{gd}}{R} + \frac{2g_mC_{gs}}{R} + \frac{g_mC_{gb}}{R} - g_m{}^2C_{db} - 2g_m{}^2C_{bs} - g_m{}^2C_{gs} - 2g_m{}^2C_{gb} + 4g_m{}^2C_{gd} - 2C_{gb}g_mg_{mb} - 2C_{gs}g_mg_{mb}) \quad (30)$$

$$s = \frac{g_m{}^2\,(g_m+g_{mb}+\frac{2}{R})}{\frac{g_m}{R}(4C_{gd}+2C_{gs}+C_{gb}) - g_m{}^2(C_{db}+2C_{bs}+C_{gs}+2C_{gb}-4C_{gd}) - 2g_mg_{mb(C_{gs}+C_{gb})}} \quad (31)$$

$$w_{tp} = \frac{(g_m+g_{mb}+{}^2/_R)}{[{}^1/_{Rg_m}(4C_{gd}+2C_{gs}+C_{gb}) - (C_{db}+2C_{bs}+C_{gs}+2C_{gb}-4C_{gd}) - {}^{2g_{mb}}/_{g_m}(C_{gb}+C_{gs})]} \quad (32)$$

Assuming, $C_{gd}=C_{gs}=C_{gb}=C_{db}=C_{bs} \approx C$

$$f_{tp} = \frac{(g_m+g_{mb}+{}^2/_R)}{2\pi C[{}^7/_{Rg_m} - 2 - 4g_mg_{mb}]} \quad (33)$$

Since the denominator factor $2\pi C[{}^7/_{Rg_m} - 2 - 4g_mg_{mb}]$ in the Eq.33 is smaller than $12\pi C$ (the denominator factor in Eq.11), therefore the bandwidth of the proposed DTMOS transistor with Self-Cascode as subcircuit is larger in comparison to the conventional DTMOS transistor. Also, there is an small increment in bandwidth by a factor ${}^2/_R$ appearing in the numerator of Eq.33. So, the bandwidth of the proposed circuit namely f_{tp}> bandwidth of the conventional circuit i.e f_t. The overall transconductance of the circuit increases. Also, when compared to the conventional DTMOS transistor, the proposed device can be operated above 0.7V due to the implementation of sub-circuit.

4. SIMULATION RESULTS FOR THE CONVENTIONAL AND PROPOSED DTMOS TRANSISTOR

The circuits have been designed using 180 nm CMOS technology from TSMC. The simulations have been carried out using SPICE to verify the predicted analytical results. The aspect ratio of the MOS transistors have been kept constant with the transistor width being equal to 260 nm and channel length 180 nm respectively. The supply voltage is maintained constant at 0.8V. The bias voltage of 0.35V is used. This low value of the supply voltage supports the idea of low voltage operation. The -3dB bandwidth of the circuit as is obtained from the analytical results is directly proportional to the transconductance.

In order to acquire the dc operation, the gate voltage was swept from 0 to 1V, and the drain current was recorded, as shown in the Fig.5. Furthermore it has been observed that the proposed circuit shows the improvement in the current driving capability by a factor of 1.87 compared with the conventional circuit in the strong inversion at the bias of V_{DD}= 0.8V.

Furthermore, the amplification capability, shown by transconductance, is shown in Fig.6.The improvement in the transconductance result from the increase of body voltage in the proposed subcircuit of Self-Cascode. By using the subcircuit the body voltage of M1 transistor is adjusted in phase with the gate voltage of M1 transistor. As the gate voltage increases, the voltage difference between the source and bulk terminals (i.e. V_{SB}) of M1 transistor also gets enhanced due to the turn on of the M2 and M3 transistors. Therefore, the threshold voltage gets decreased with the increase in body voltage and hence low voltage will be required to turn the transistor ON as shown in Fig.7. The Fig.8 shows the output characteristics of the proposed DTMOS structure which clearly shows the various region of operations.

The Fig.9 shows the transient input which is given as input to the proposed DTMOS to verify its behavior with time. Fig.10 and Fig.11 depicts the transient ouptput across the conventional and proposed DTMOS transistor. Fig.12 shows comparison of transient outputs and it is observed that the output range of the proposed DTMOS has increased appreciably.The output range of the proposed DTMOS transistor has increased by a factor of about more than 4 times which is a very good improvement.

Bandwidth is a very important parameter in high frequency circuits. The demand for the low voltage and low power wideband devices is increasing in analog applications. Hence many new and alternative techniques are coming up for enhancement of the bandwidth. As technology scaling is

increasing, use of ultra low supply voltage degrades the analog performance of the nanoscale devices because of the reduced transconductance ratio. The -3dB frequency of conventional DTMOS circuit is 326.038 MHz as shown in Fig.13 and the -3dB frequency of the proposed DTMOS circuit is 754.37 MHz as is shown in Fig.14. Fig.15 depicts the simulated AC response of the proposed DTMOS. Thus the proposed concept of tying the gate body terminal with Self-Cascode subcircuit in their path comes up with the bandwidth extension ratio (BWER) of 2.31 in proposed DTMOS circuit.

The effect of temperature on the analog circuits often plays a very important role on the circuit performance. It is observed from the Fig.16 that the current driving capability of the proposed DTMOS transistor degrades with the increase in the temperature. The Fig.17 shows the simulated results for the proposed DTMOS transistor by varying the gate voltage V_{GS} and observing the output current variations with the temperature. The different curves are plotted for different values of the temperature and the value of the drain current reduces with the increment in temperature. Thus the proposed DTMOS transistor is sensitive to temperature variations.

Minute random variations generally occur in the circuit during the manufacturing, that results in the behavioral differences among the devices that are identically designed. These variations or mismatches in the device .are quite usually ignored and are considered as non-relevant. Also it is not so surprising as it is quite tedious to predict the behavior of any non-trivial circuit analytically as the mismatch errors from the individual devices accumulate. However to physically understand the device mismatch aspect many quantitative models exist that predict the device mismatch accurately. Monte carlo simulation is a very effective method to understand and find out how the mismatch of individual device of a circuit may accumulate and affect the circuit as a whole. This can be achieved by considering a large number of circuit instantiations. Circuit devices have also each been randomized individually according to the mismatch model of the particular device type.

Fig.18 shows the behavior of proposed DTMOS transistor with 5% variation in the degenerate resistor. From the results it is observed that the proposed DTMOS transistor is robust to resistor value variations. Fig.19 shows the bar graph representation of the Monte Carlo simulations.

Table 1 summarizes the results for c0nventional and proposed conventional DTMOS transistors.

Table 1. Comparison of conventional and proposed DTMOS transistor for various parameters

Parameters	Conventional DTMOS	Proposed DTMOS
CMOS technology	TSMC 0.18 um	TSMC 0.18 um
Supply voltage	0.8V	0.8V
Bandwidth (in Hz)	326.038 M	754.37 M
f_T equation	$\frac{(g_m+g_{mb})}{12\pi C}$	$\frac{(g_m+g_{mb}+{}^2/_R)}{2\pi C[{}^7/_{Rg_m}-2-4g_mg_{mb}]}$
g_m(inA/V)	1.6731 m	2.6646 m
I_D	1.3373 mA	2.5137 mA
Power dissipation	2.63 x 10^{-10} W	3.51 x 10^{-10} W

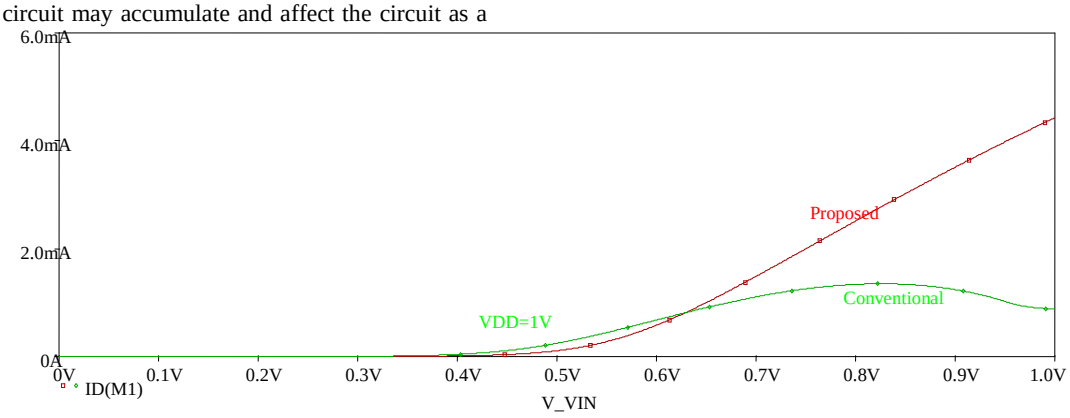

Fig 5: Drain current plot by varying Vgs in the proposed and conventional DTMOS (x-axis: input voltage V_{gs}, y-axis: output current I_D)

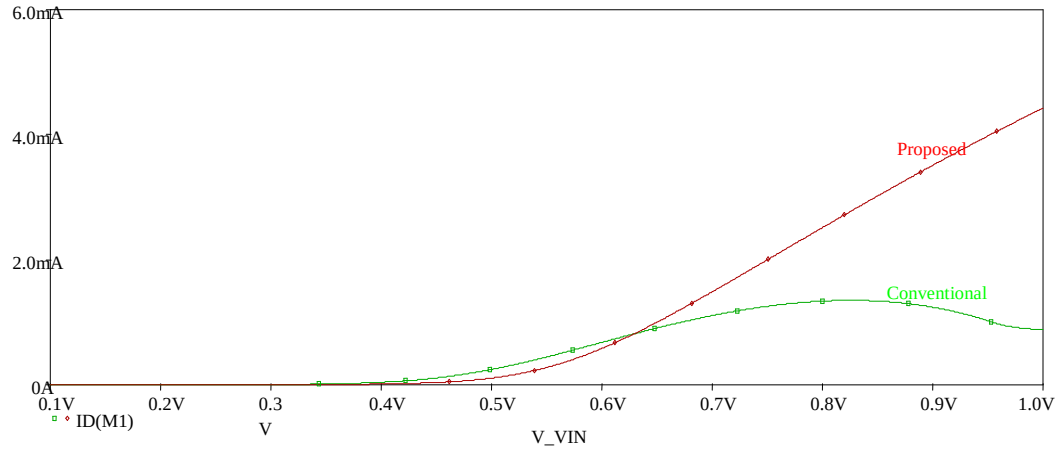

Fig 6: Transconductance variation of the proposed and conventional DTMOS (x-axis: Gate -Source voltage V_{gs} y-axis: transconductangeg_m)

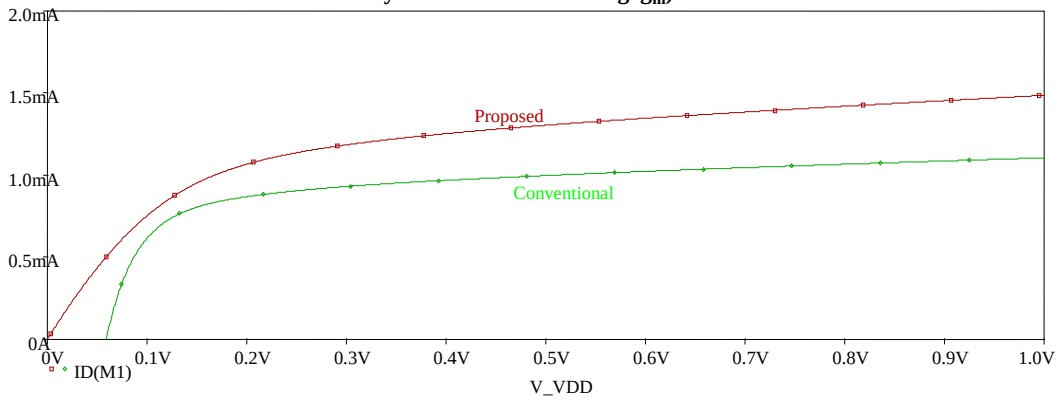

Fig 7: Output characteristics of the proposed and conventional DTMOS (x-axis: supply voltage $V_{DD,}$ y-axis: Drain current I_D)

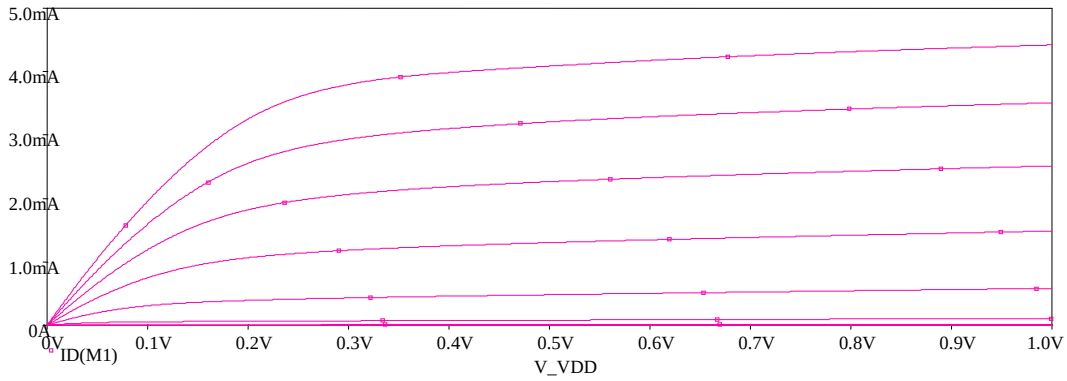

Fig 8: Output characteristics of the proposed DTMOS (x-axis: supply voltage $V_{DD,}$ y-axis: Drain current I_D)

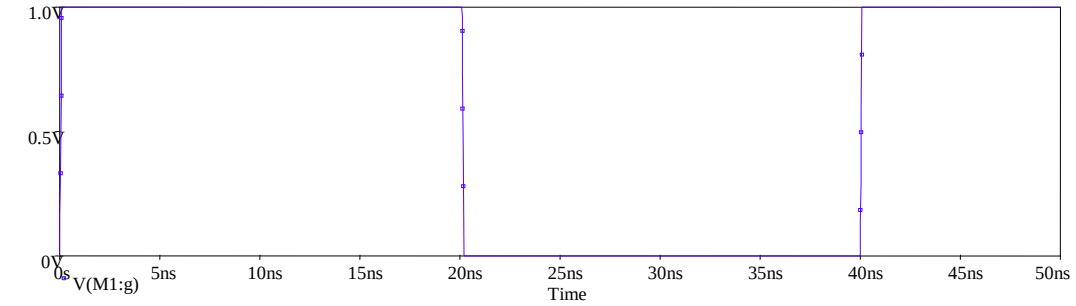

Fig 9: Transient input provided to the proposed DTMOS (x-axis : time, y-axis: Input voltage)

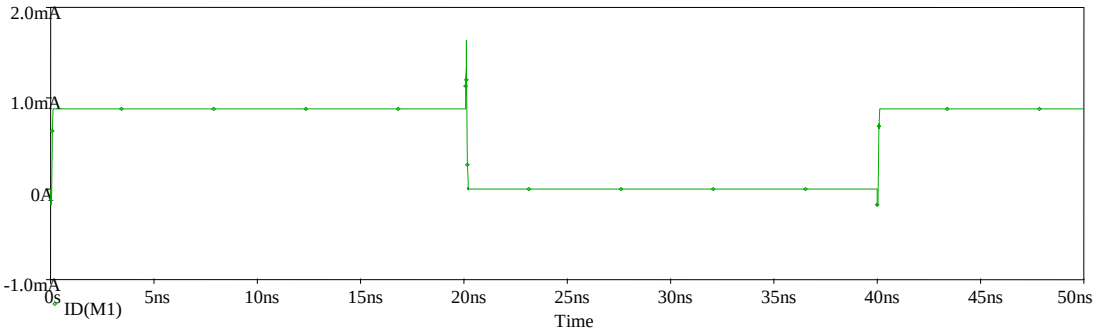

Fig 10: Transient output across the conventional DTMOS (x-axis : time, y-axis: output current)

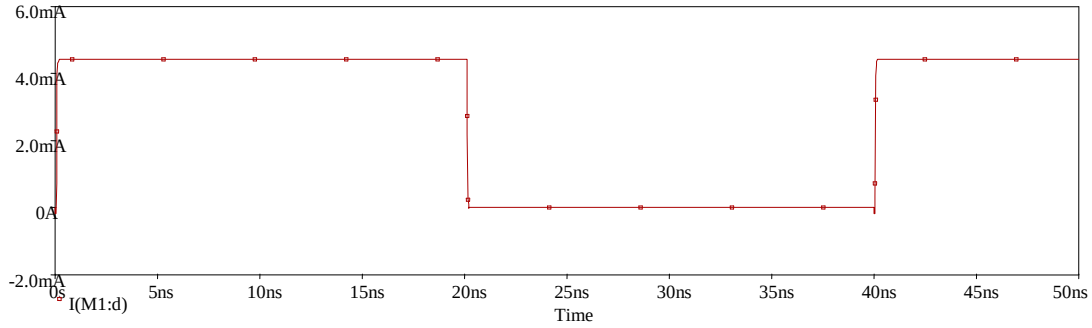

Fig 11: Transient output across the proposed DTMOS (x-axis : time, y-axis: output current)

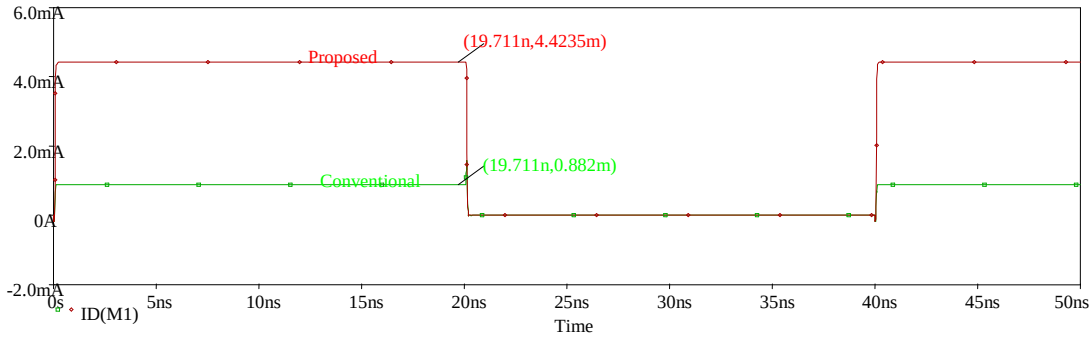

Fig 12: Comparison of the transient output across conventional and proposed DTMOS (x-axis : time, y-axis: output current)

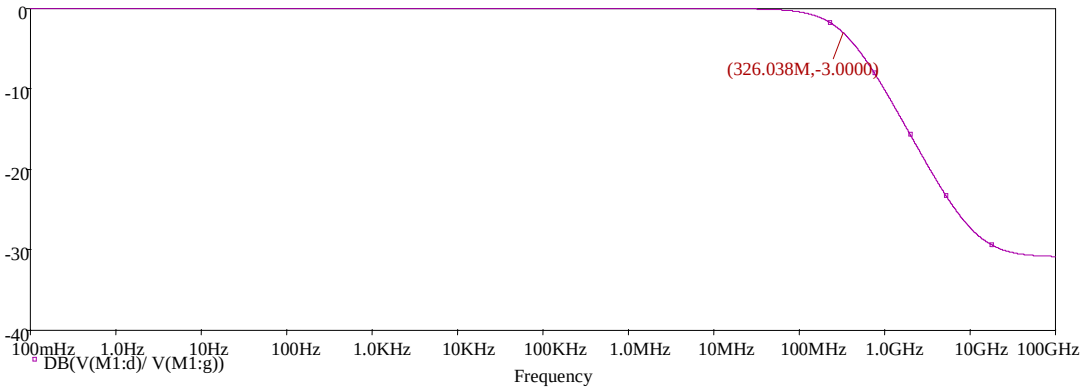

Fig 13: Bandwidth of the conventional DTMOS (x-axis: frequency variations y-axis: gain in dB)

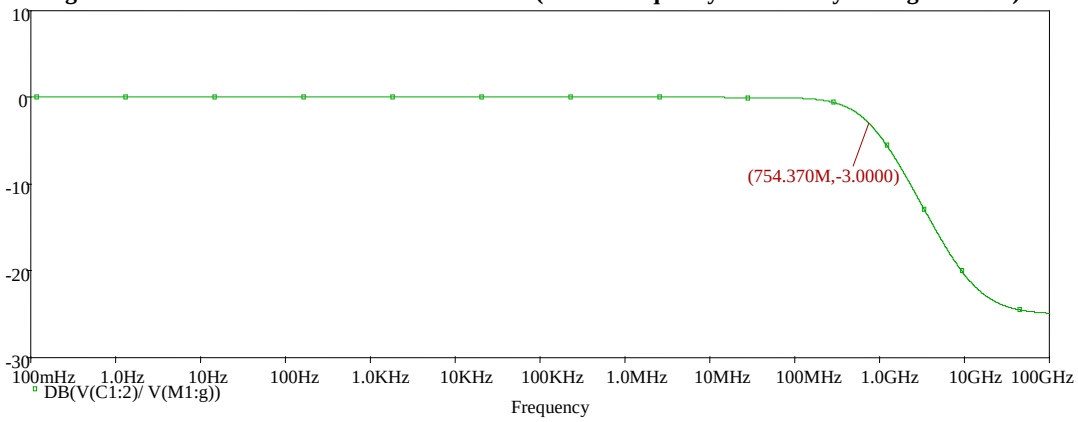

Fig 14: Bandwidth of the proposed DTMOS (x-axis: frequency variations, y-axis: gain in dB)

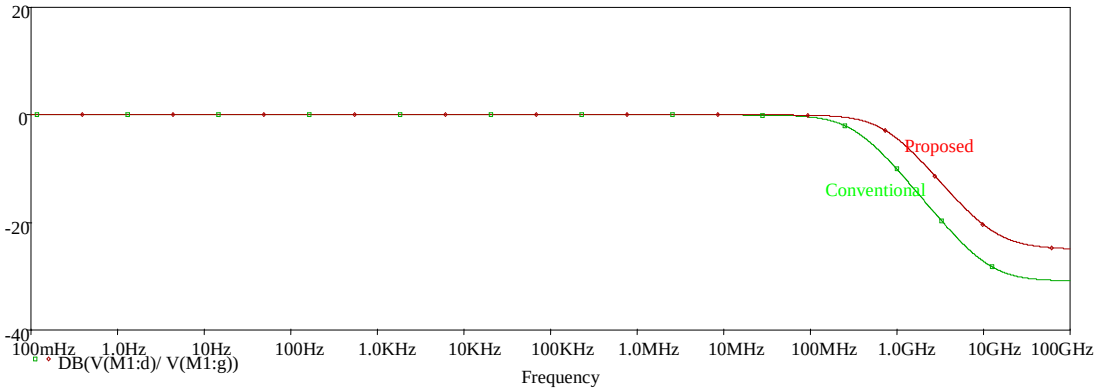

Fig 15: Comparison of bandwidth of conventional and proposed DTMOS (x-axis: frequency variations, y-axis: gain in dB)

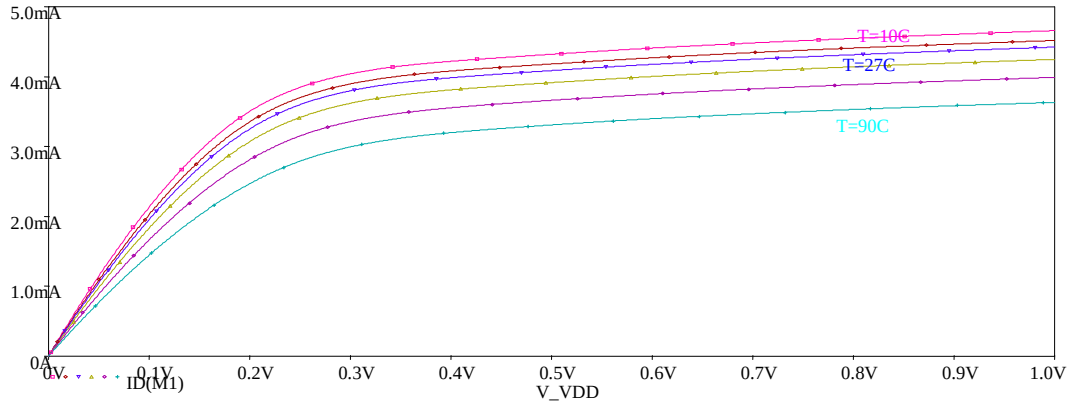

Fig 16: $I_D$vsV_{DD} variations with temperature (x-axis: supply voltage V_{DD}, y-axis: drain current I_D)

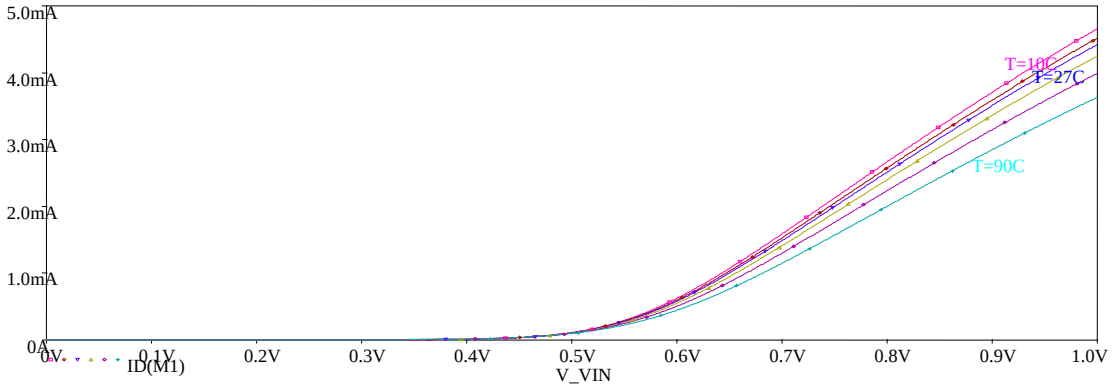

Fig 17: I_D versus V_{GS} variations with temperature (x-axis: supply voltage V_{GS}, y-axis: drain current I_D)

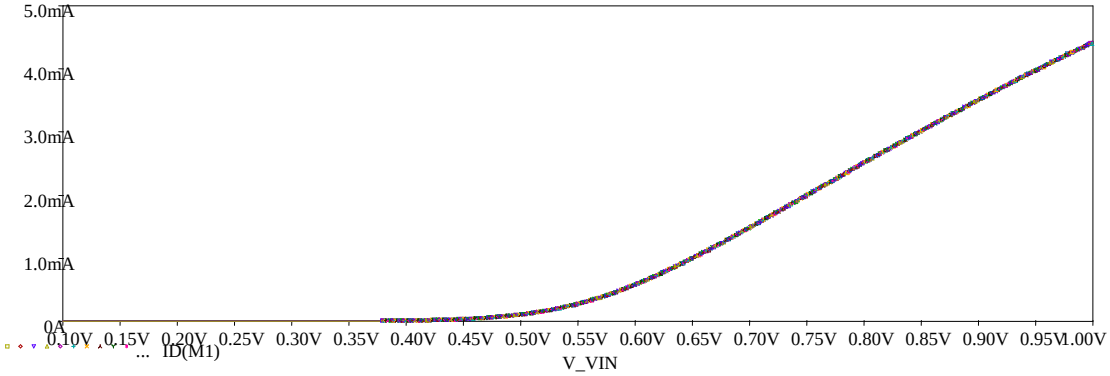

Fig 18: Monte carlo simulation by providing 5% tolerance to the degenerate resistor R

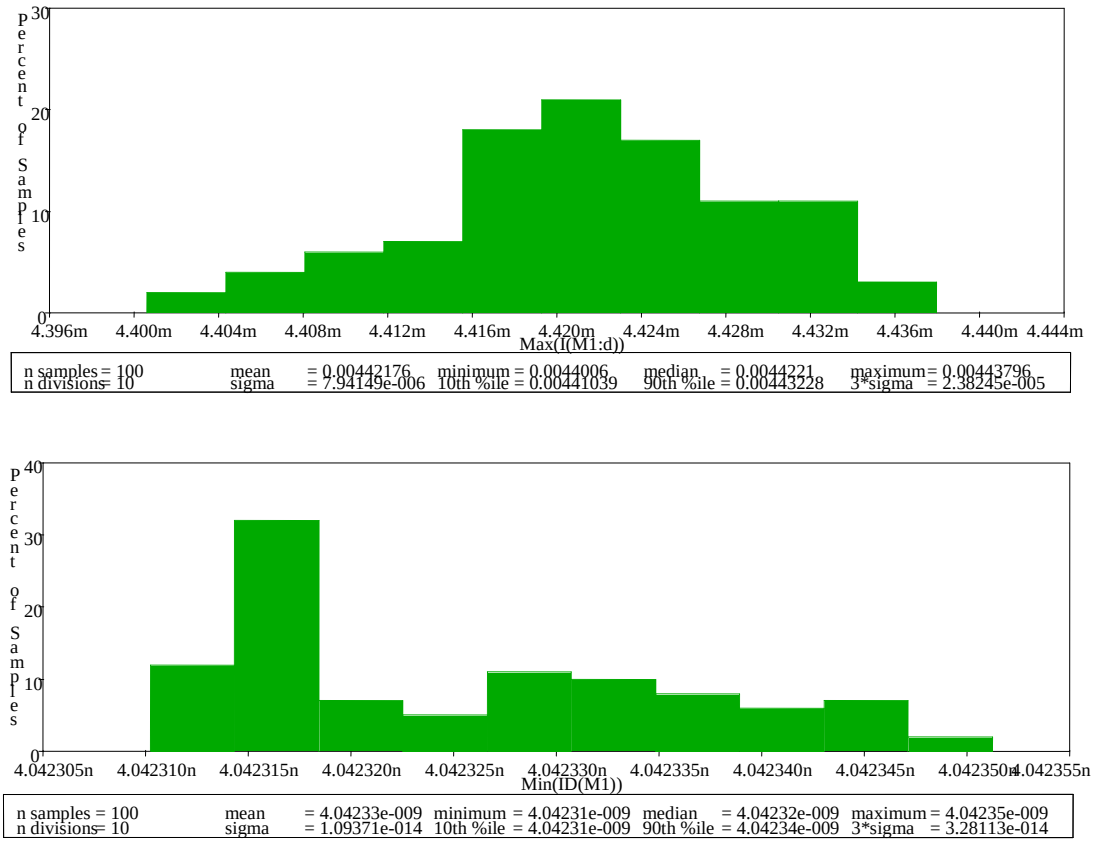

Fig.19 Bar graph representation of the Monte Carlo simulations

5. APPLICATION OF PROPOSED DTMOS TRANSISTOR

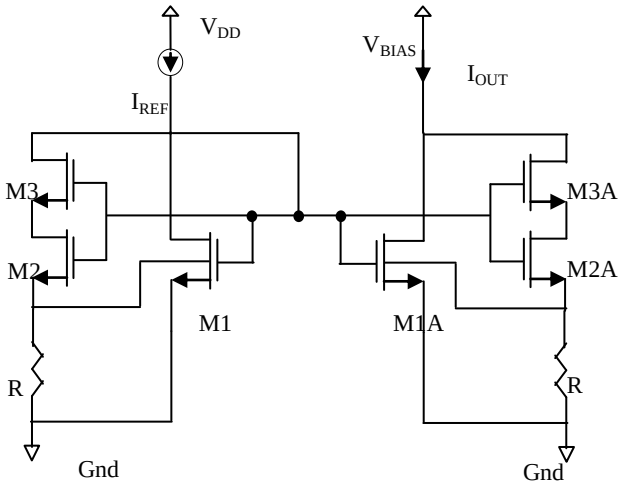

Fig 20: Proposed Current mirror

Current mirrors are one of the most versatile building blocks in analog signal processing and current mode circuits. They perform various functions like current amplification, biasing and active loading etc.[14]. The design of low voltage current mirror involves different conflicting design specifications like noise, bandwidth, input and output impedances, power dissipation, accuracy, THD for instance, while only three design MOS transistor parameters namely DC current, Width, Length are available for designer. Modern VLSI systems now operating from single 1.5V supplies and dropping, require high performance current mirrors that can operate with low power supply voltages in applications where high data rates and large bandwidth are required. At a given bias point, the power-speed ratio of the current mirror circuit is fixed by the DC accuracy requirement . Also there is a tradeoff between the bandwidth, accuracy and power consumption which is set by technology parameters [15]. To verify the usefulness of the proposed DTMOS transistor, a current mirror is designed shown in Fig.20.

The DC response of proposed current mirror is shown in Fig.21.The frequency response of proposed current mirror is shown in the Fig.22. The bandwidth of the conventional current mirror is 2.9808 GHz which increases to 4.3636 GHz in the proposed current mirror.

The most important analog building block is a differential pair. It is the input stage of an operational amplifier and most integrated filters. The usefulness of the differential pair stems from two key properties. First, cascades of differential pairs can be directly connected to one another without interstage coupling capacitors. Second, the differential pair is primarily sensitive to the difference between two input voltages, allowing a high degree of rejection of signals common to both the inputs. Hence differential amplifier has become dominant choice in low noise and high performance analog and mixed signal circuits. The differential amplifier with the proposed DTMOS transistor is as shown in the Fig.23. As is clear from the figure the transistor M1 and M1A have an additional self-cascode subcircuit unit with them.

Fig.24 depicts the simulation results for the DC response. The maximum output swing in case of the conventional

differential amplifier is 652.024 mV which increases to 873.411 mV in case of the proposed Differential amplifier. Clearly a significant increase of 221.387 mV is observed in the maximum output swing.

Frequency response of the proposed and conventional Differential amplifier is shown in the Fig.25. For the differential AC input of 100 mV the -3dB frequency is 1.5541 MHz for the conventional differential amplifier and the -3dB frequency for the proposed differential amplifier is 5.1532 MHz achieving a BWER of 3.316. Thus an appreciable increment in the transition frequency is achieved. Table 2 summarizes the improvement in bandwidth obtained in conventional and proposed circuits.

Table 2. Bandwidth comparison of conventional and proposed applications

Circuit	**Bandwidth of Conventional circuit(in Hz)**	**Bandwidth of Proposed circuit (in Hz)**	**BWER**
Differential Amplifier	1.5541M	5.1532M	3.316
Current mirror	2.9606G	4.3636G	1.474

6. CONCLUSION

The growing demand of low voltage low power wideband circuits in analog signal processing necessitates new and alternative techniques for bandwidth enhancement. As technology is scaling down, the analog performance of nanoscale devices is getting impaired by the ultra low supply voltages adopted and by the reduced g_m/g_{ds} maximum achievable values. In this paper a new technique to increase the bandwidth of current mirror and differential amplifier using DTMOS transistor with self-cascode subcircuit has been proposed. The proposed approach increases its transconductance and thereby improving bandwidth. The current mirror and differential amplifier using proposed DTMOS transistor shows excellent frequency response when compared to the conventional versions. Although use of additional transistor may increase slightly the power consumption of circuit but advantage obtained in terms of higher bandwidth is more significant. Thus the proposed circuits could be very well applicable for low power RF analog domains.

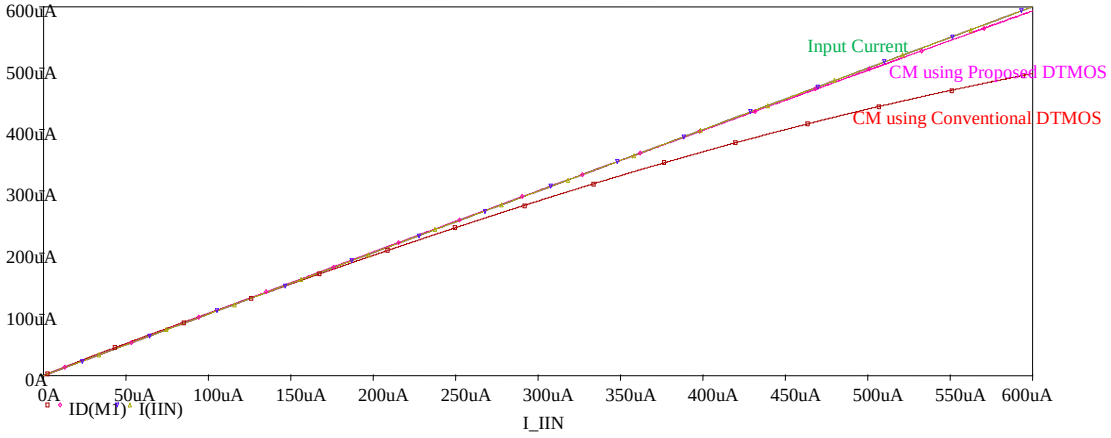

Fig 21: DC response of Proposed Current mirror

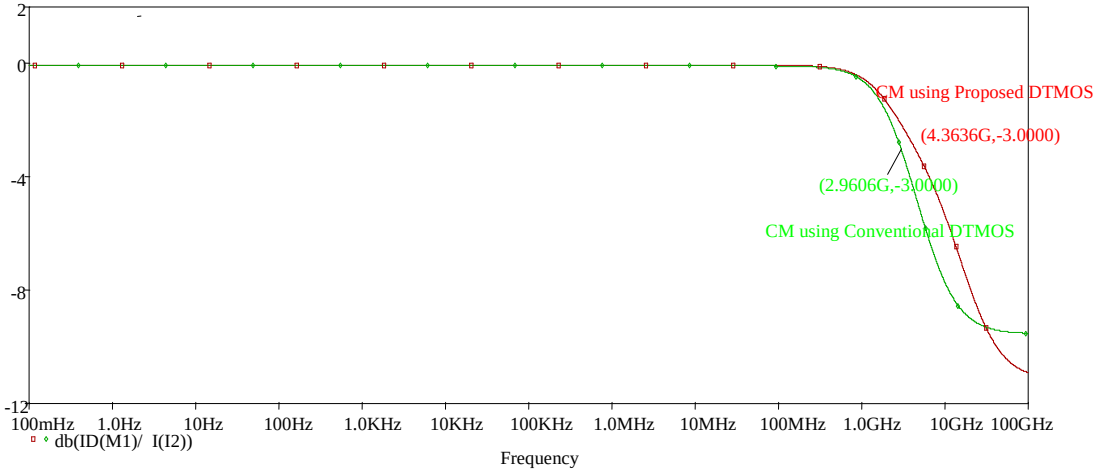

Fig 22: Frequency response of proposed current mirror

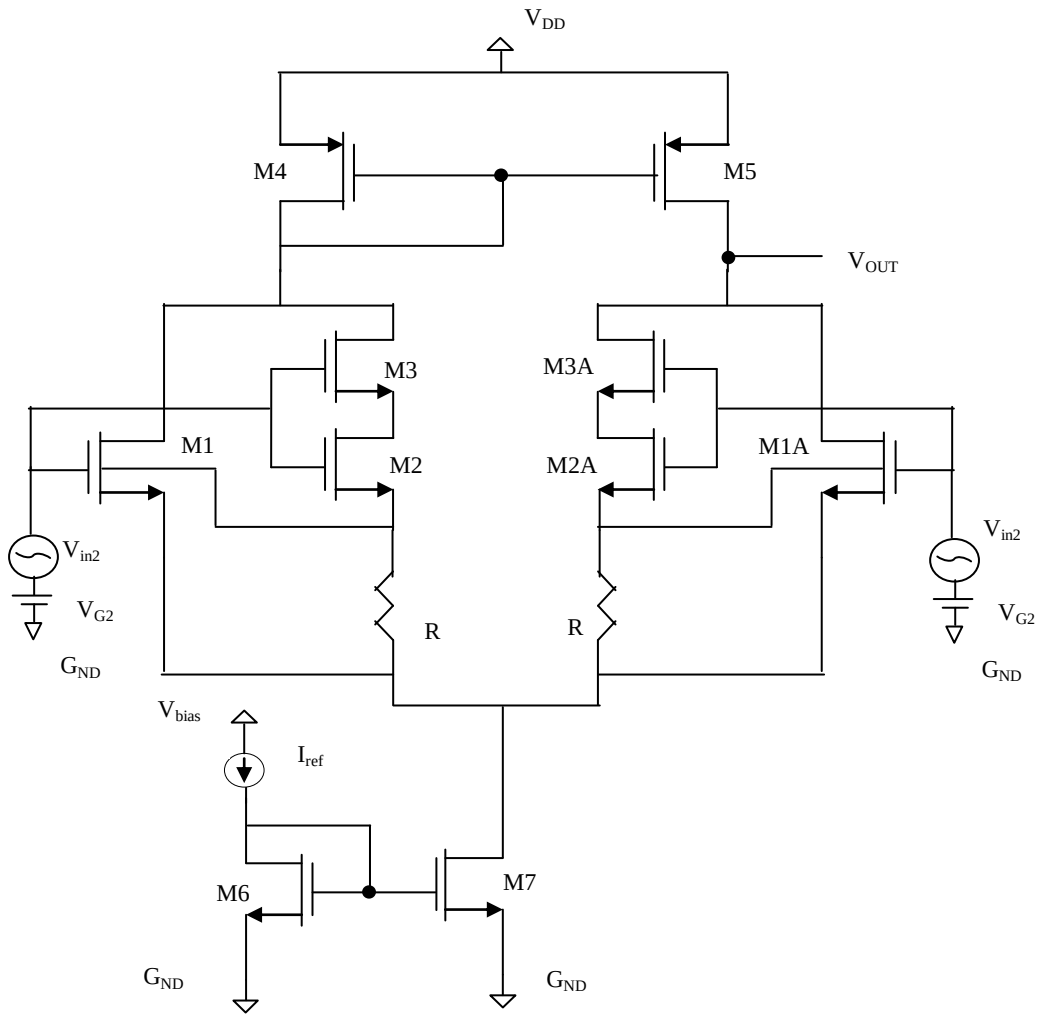

Fig 23: Proposed Differential amplifier

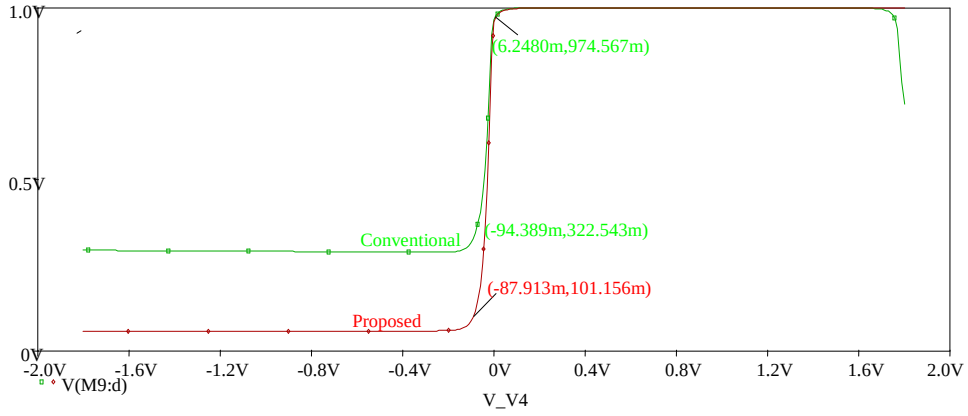

Fig 24: DC response of proposed differential amplifier

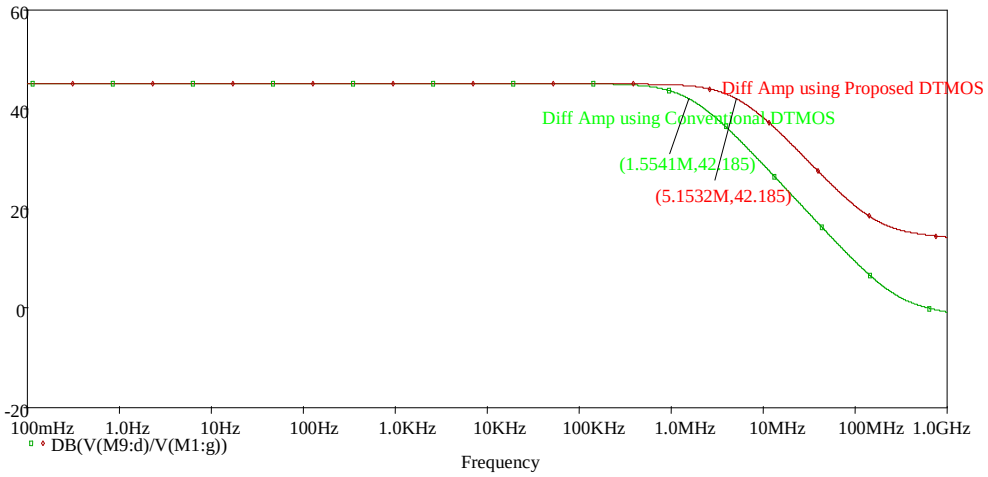

Fig 25: Bandwidth comparison of proposed and conventional differential amplifier

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