FinFET based 6T SRAM Cell for Nanoscaled Technologies

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ABSTRACT
FinFET is a non planar modeling device for small size transistors (less than 45nm) will replace traditional planar MOSFETs because of superior ability to control short channel effects, off-state leakage current, power dissipation and propagation delay. Static random access memories (SRAMs) consume nearly 94% of chip area in most present system-on-chip (SoC) circuits. In this paper, a standard 6T SRAM cell has been designed using dual gate FinFET transistors and its performance for read/write operation is analyzed in terms of average power consumption, propagation delay, power delay product (PDP) and static noise margin (SNM) for nanoscaled technologies. A comprehensive comparison is carried out with conventional 6T CMOS SRAM cell for 45nm, 32nm and 16nm nanoscaled technologies. A reduction in power delay product by 87.5%, 88.8% and 99.1% in read operation and 90.4%, 89.2% and 96.9% in write operation of FinFET based SRAM cell at 45nm, 32nm and 16nm technology nodes respectively as compared to 6T CMOS SRAM cell. Also an improvement in static noise margin by 27.5%, 31.5% and 8.9% of FinFET based SRAM cell is obtained at 45nm, 32nm and 16nm technology nodes respectively.

Keywords
CMOS, FinFET, SRAM, DRAM, SNM, PDP, SoC, RDF, SCE

1. INTRODUCTION
Standard 6T SRAM cell is mostly preferred in memory designs as it fulfils stringent performance requirements and also the read & write operations are very simple. A 6T SRAM cell stores 1-bit of data in two cross coupled inverters forming a latch and employs two transistors for read and write operation. Word-line is used to activate access transistor which facilitate the communication of internal cell nodes with input/output ports of the cell called bit-lines. For read and write stability, sizing of the transistors has to be done carefully. During read operation bit-lines are driven high and low respectively by two cross-coupled inverters in 6T SRAM cell which improves SRAM bandwidth as compared to DRAM. 6T-SRAM cell may be designed at suitable technology nodes by using CMOS, FinFET and/or CNTFET devices [4-6].

1.1 SRAM Design Tradeoffs
1.1.1 Area and Yield
The most important properties of memory design are its density and functionality. Functionality for large memories is secured by providing good noise margin between outputs. The noise margins can be reduced by proper sizing of the device. Also by selecting threshold voltages and supply voltage the functionality can be improved. Upsizing of transistors decreases density of memory as cell area increases [1-3].

1.1.2 Read and Write Stability
The minimum voltage that can be reached during read operation is called as read voltage is determined by division of voltage between pull down transistor and access transistor. Read stability can be confirmed by low access transistor driving strength which decreases read voltage. In write operation, the maximum voltage that can be reached is called write voltage which is determined by division of voltage between access transistor and pull up transistor. Write stability can be confirmed by strong access transistor driving strength which decreases write voltage [1-3].

1.1.3 Speed and Leakage Current
Low leakage power is always requirement of SRAM cell which increases speed of operation and cell performance. Speed can be increased by providing low threshold voltage but as a result it also increases leakage power of the device. As the scaling increases scaling of voltage leads to less threshold voltage which will increase speed and also leakage power. To overcome leakage power high threshold voltage can be used but performance degrades by unacceptable margin [1-3].

2. FinFET STRUCTURAL DETAILS & PROPERTIES
FinFET technology has been outperforming CMOS technology below 32nm and emerged as successful replacement for it. This trend is expected to continue at least for 3 to 4 technology generations [1-3].

FinFETs offer greater electrostatic control over the channel due to its multigate structure. This greatly enhances the short channel behaviour in nanoscaled technologies. FinFET transistors use light body doping to minimize random dopant fluctuations (RDF). This further minimizes the process variation and Ion/Ioff current. Due to these beneficial features and device characteristics FinFETs are becoming better alternate for conventional bulk FETs in nanoscaled technologies [8-12]. Figure 1 shows the 2D structure of a Double Gate (DG) FinFET.

2.1 Structural Parameters
The important structural parameters of a Double Gate (DG) FinFET transistor are depicted in figure 2.

L_{GF}, L_{GB}: Physical front- and back-gate lengths defined by the spacer gap.

H_{FIN}: Height of silicon fin decided by the distance between top gate and buried oxides.

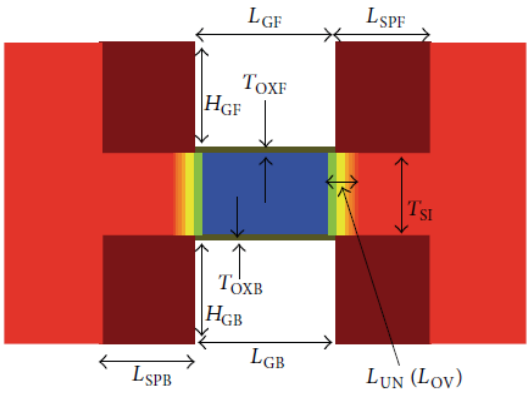

Fig. 1 2D FinFET Structure [17]

T_{SI}: Thickness of silicon fin determined by the space between front and back gate oxides.

T_{OXF}, T_{OXB}: Front- and back-gate thickness of oxide layer.

H_{GF}, H_{GB}: Front- and back-gate thickness.

L_{SPF}, L_{SPB}: Front- and back-gate spacer thickness.

L_{UN}: Gate-drain/ source underlap.

$N_{S/D}$: Source/drain doping.

N_{BODY}: Body doping.

FP, GP: Fin pitch, Gate pitch

W_{fin}: Geometrical channel width. It is determined by $W_{fin}= 2H_{fin}+ T_{si}$.

2.2 FinFET Features

The following features of FinFET make it an ideal candidate for SRAM design in nanoscaled technologies:

- Thin body suppresses short channel effects (SCE).
- Lesser channel doping provides better SCE control and also reduces process variations arising due to statistical dopant fluctuation effects.
- Better carrier mobility, gate leakage currents and device reliability due to light body doping.
- Steeper sub-threshold slope and lower junction and body capacitance.
- Lower mobility degradation due to lower capacitance and improved logic delay than the planar bulk devices.
- The provisioning of separate front and back gates allows improved control over the channel current.
- By using high-k gate dielectrics also it will be difficult for conventional planar transistor to scale effectively.

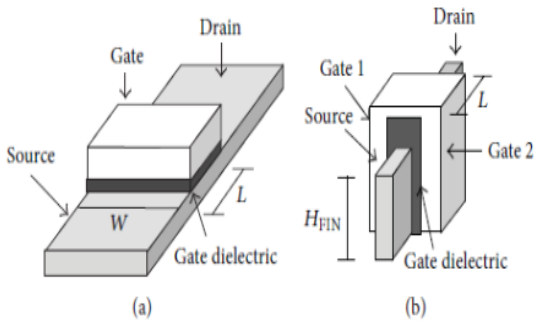

Fig. 2 Structural comparison between (a) planar MOSFET and (b) FinFET [1]

Figure 2 shows structural comparison between conventional MOS transistor and non-planar FinFET transistor.

3. 6T SRAM CELL OPERATION

3.1 Standby Mode

Word line is not asserted in this mode *(WL=0)*, so access transistors M5 and M6 will be *off* and no data will be accessed by the bit-lines as shown in figure 3. The cross-coupled inverters will continue to feedback each other and hold the data in the latch as long as it is connected to the supply [12-15].

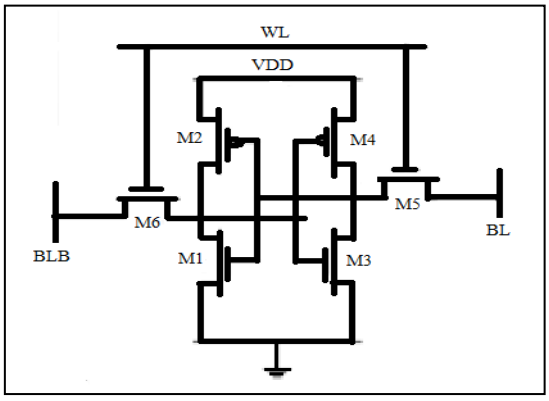

Fig. 3 6T FinFET SRAM cell

3.2 Read Mode

Word line is asserted *(WL=1)*, which enables both the access transistor and connect cell from the bit lines *BL* and *BLB*. In read operation value stored in the nodes Q and QB are transferred to respective bit-lines *BL* and *BLB*. If *1* is stored at node *Q* then M2 and M4 will be *On* and M1 and M3 will be *Off*. *BLB* will be discharged through the driver transistor M4 and BL will be pulled up through the load transistor M2 toward V_{DD} [12-15].

3.1 Write Mode

Word line is asserted *(WL=1)*. If *1* is stored in the cell and *0* is to be written then bit line *BL* will be lowered to *0V* and *BLB* is raised to *VDD*. For proper functioning of SRAM cell i.e. read and write operation certain aspects have to be taken in mind. These design issues decide the stability of read and write operations [12-15]. The figure 4 and 5 depicts SRAM cell configurations during read and write operations.

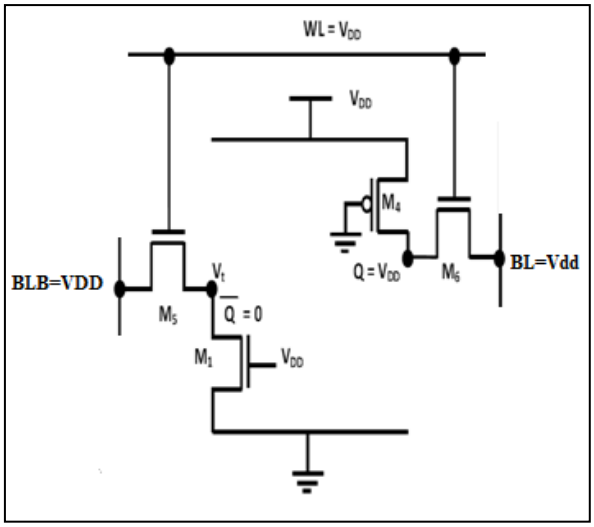

Fig. 4 SRAM cell read operation

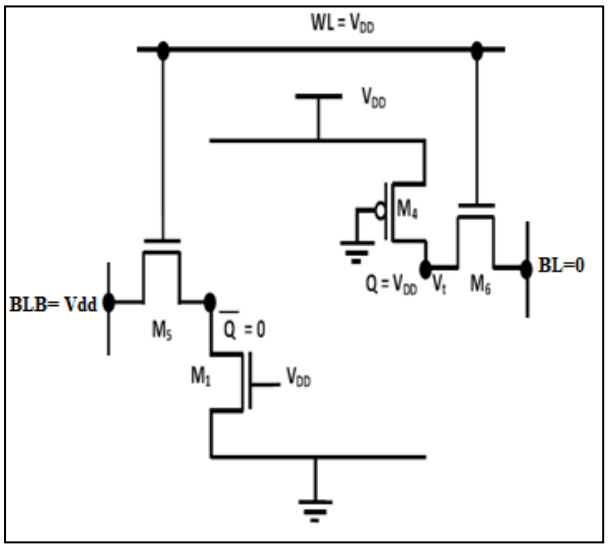

Fig. 5 SRAM cell write operation

- ***Cell ratio***: It is defined as the ratio of the W/L ratio of driver transistor to W/L ratio of access transistor. It is given as-

$$CR = \frac{\frac{W_1}{L_1}}{\frac{W_5}{L_5}} \text{ or } CR = \frac{W_1}{W_5} \text{ when L is fixed}$$

- ***Pull-up ratio***: It is defined as the ratio of the W/L ratio of load transistor to the W/L of access transistor. It is given as-

$$PR = \frac{\frac{W_4}{L_4}}{\frac{W_6}{L_6}} \text{ or } CR = \frac{W_4}{W_6} \text{ when L is fixed}$$

4. PERFORMANCE PARAMETERS OF SRAM

4.1. Power dissipation

Power dissipation is the major factor that we dealt with memory. FinFET technique helps us in reducing the power consumption in SRAM circuits.

4.2 Delay

Delay calculation is the major section of any digital circuit. As the power supply is scaled down, delay is increased. This delay must be not so much high that it would affect the working of the normal circuits.

4.3 Power-delay-product (PDP)

The power-delay-product (PDP) is the product of the power consumed and the propagation delay of the circuit. It should ne minimum f or better performance and reliability.

4.4. Static Noise Margin (SNM)

Static noise margin mainly depends on threshold voltage used in 6T SRAM cell. High threshold voltage leads to small drive current due to which write operation becomes difficult and thus SNM increases. So, to reduce the power of cell with improved stability, a high threshold voltage can be used, but performance degrades. FinFET transistors are better in this regard as it provide higher drive current with larger threshold voltage due to which high noise margin and good write stability is achieved.

5. SIMULATION RESULTS

6T FinFET SRAM cell has been designed and its performance has been analyzed at 45, 32, 20, 16, 14, 10 and 7nm nanoscaled technologies. The H-Spice simulator is used for simulation purposes and predictive technology model parameters are used. Table 1 lists important FinFET parameters used for various nanoscaled technologies. These standard values have been taken for the analysis of 6T FinFET SRAM cell. Table 2 lists average power, delay and power delay product (PDP) calculated for read and write operations. Figures 6, 7 and 8 show bar-graph plots of the average power, propagation delay and power delay product for read and write operations. It has been observed that as technology scales down, average power of the 6T FinFET SRAM cell increases, delay is improved and power delay product also improves significantly for read and write operations.

Table 1: Parameters for different technology nodes

	Technology Node						
Parameters	45	32	22	16	14	10	7
VDD (V)	1	0.9	0.9	0.85	0.8	0.75	0.7
L_{GF} (nm)	45	32	22	16	14	10	7
L_{GB} (nm)	45	32	22	16	14	10	7
T_{OXF} (nm)	1.5	1.4	1.4	1.35	1.3	1.2	1.15
T_{OXB} (nm)	1.5	1.4	1.4	1.35	1.3	1.2	1.15
T_{SI} (nm)	8.4	8.6	10	9	8	7	7
H_{FIN} (nm)	60	40	28	26	23	21	18
H_{GF} (nm)	60	40	28	26	23	21	18
H_{GB} (nm)	60	40	28	26	23	21	18

Table 2: Average power, delay and PDP of FinFET SRAM cell at different technology nodes

Parameters	Read operation				
Technology node (nm)	20	16	14	10	7
Power (nW)	21.77	17.57	14.24	12.07	9.45
Delay(ps)	8.46	3.90	2.78	2.02	1.51
PDP (aJ)	0.18	0.068	0.039	0.024	0.0143
	Write operation				
Technology node (nm)	20	16	14	10	7
Power (μW)	6.15	4.59	1.04	.0143	.0109
Delay(ps)	8.840	7.417	6.426	3.036	2.640
PDP (aJ)	54.383	34.066	6.728	0.043	0.028

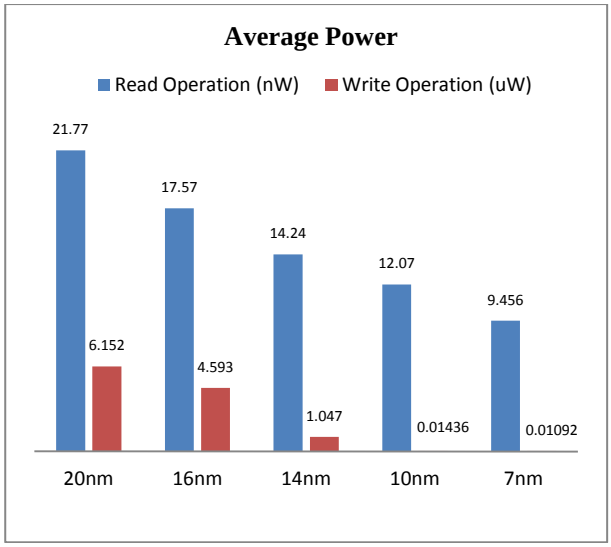

Fig. 6 Average power calculation at different technology nodes

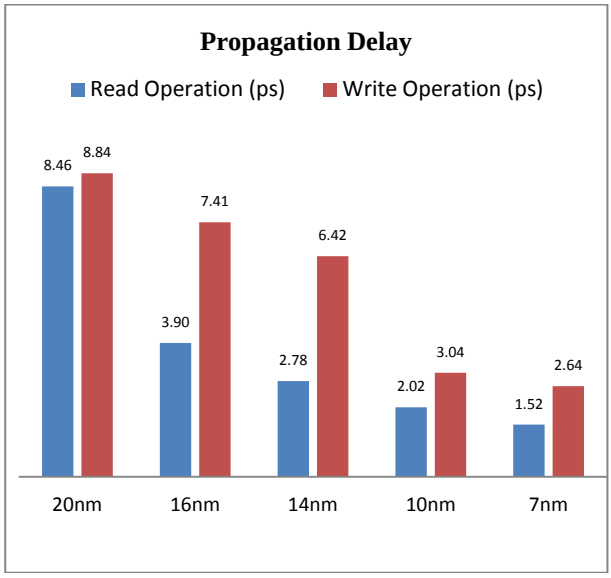

Fig. 7 Propagation delay calculation at different technology nodes

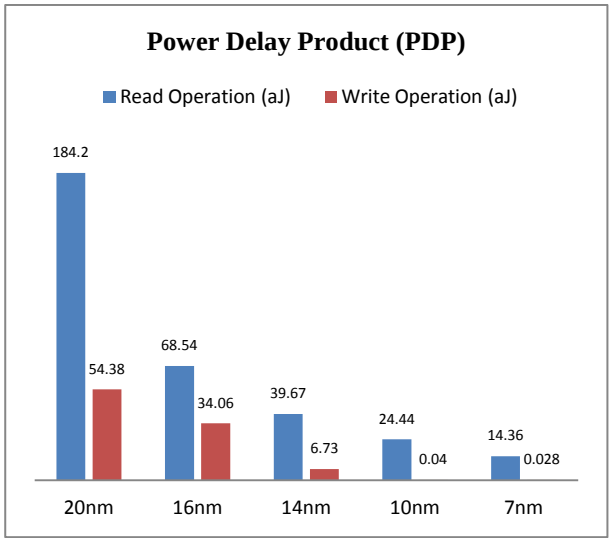

Fig. 8 PDP calculation at different technology nodes

5.1 Comparison of results

Average power for read and write operation has been shown a decrease in FinFET 6T-SRAM cell as compared to conventional 6T CMOS SRAM cell at 45nm, 32nm and 16nm technologies. The percentage change in the average power is given in the table 3 below. Fig. 9 and 10 show bar-graph comparison of average power for read and write operations in CMOS and FinFET 6T SRAM cell.

Table 3: Average power comparison results

	45nm	32nm	16nm
Read operation	3.075%	57.263%	90.7133%
Write operation	1.778%	59.028%	95.68%

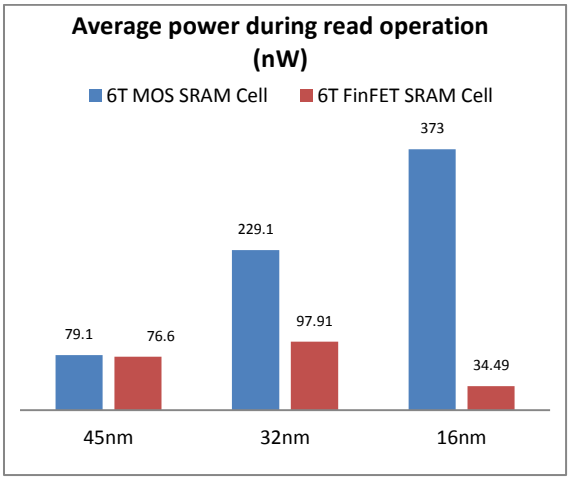

Fig 9 Average power during read operation

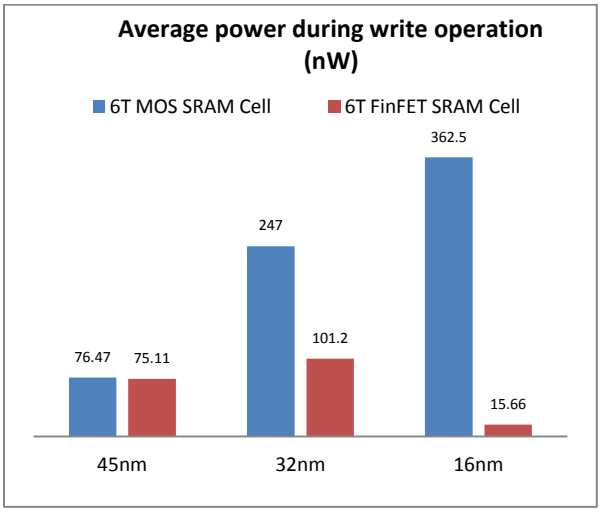

Fig 10 Average power during write operation

Figure 11 and 12 show bar-graph comparisons of propagation delay for read and write operations for CMOS and FinFET 6T SRAM cells. Fig. 13 and 14 show comparison of power delay product for read and write operations for CMOS and FinFET 6T SRAM cells.

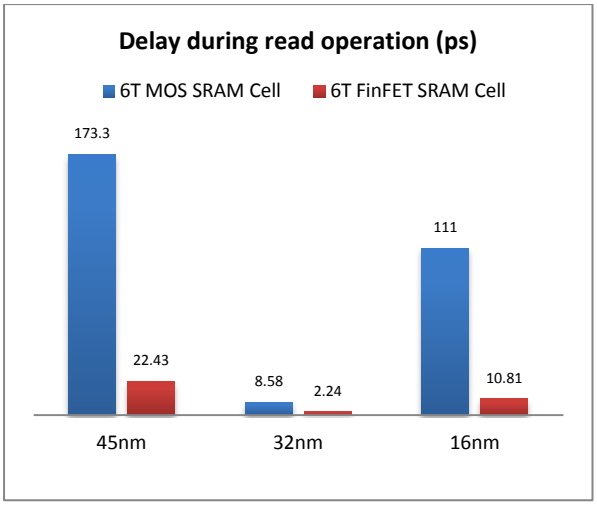

Fig 11 Propagation delay for read operation

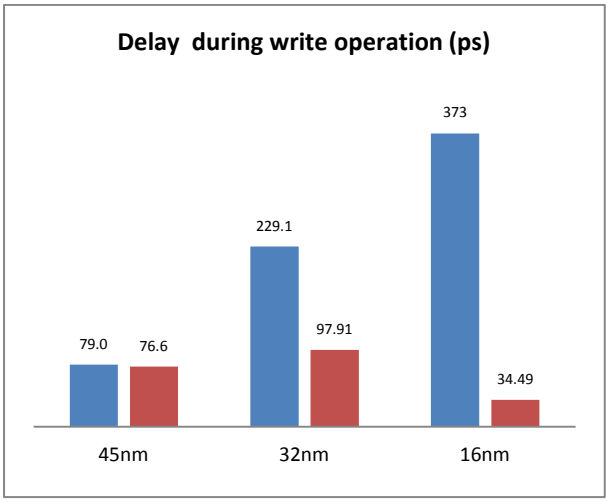

Fig 12 Propagation delay for write operation

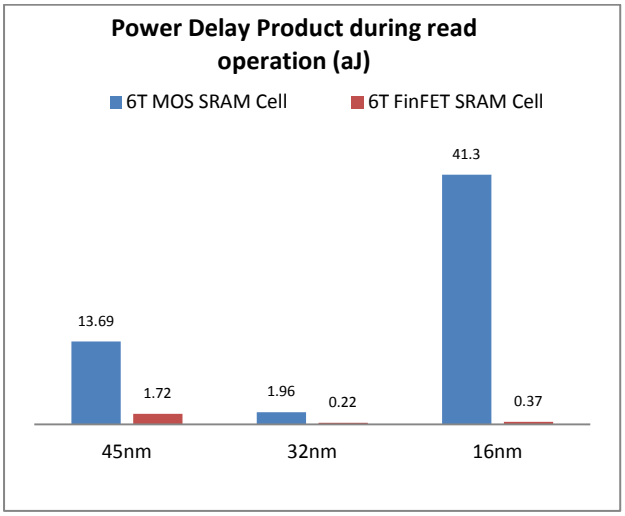

Fig 13 Power delay product for read operation

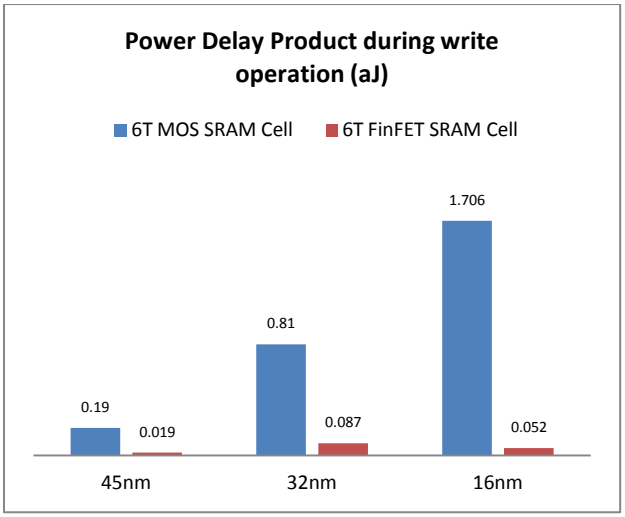

Fig 14 Power delay product for write operation

Delay for read and write operation has been calculated and a decrease has been observed in FinFET SRAM cell as compared to conventional 6T CMOS SRAM cell. The percentage change in the delay is given in table 4.

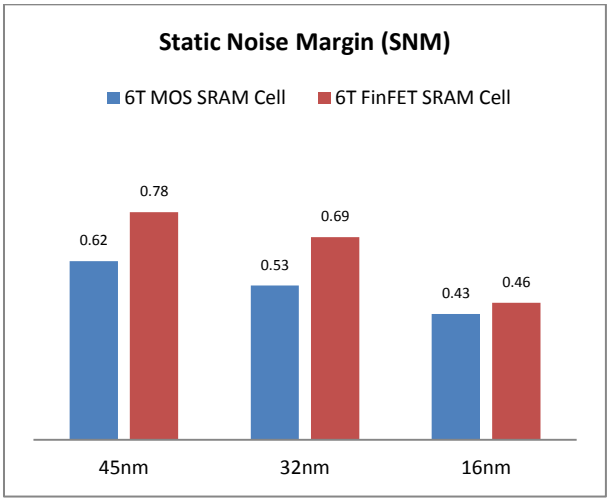

Fig 15 Static noise margins for FinFET and CMOS 6T SRAM cells

Table 4: Propagation delay comparison results

	45nm	32nm	16nm
Read Operation	87.057%	73.916%	90.2612%
Write Operation	90.195%	73.639%	29.934%

PDP is the product of average power and delay. PDP of SRAM cell has to be minimum for better performance and reliability. Non-planar 6T FinFET SRAM cell has shown a decrease in PDP as compared to planar 6T SRAM CMOS Cell. The percentage change in the PDP is given in table 5.

Table 5: Propagation-delay-product (PDP) comparison results

	45nm	32nm	16nm
Read Operation	87.455%	88.852%	99.084%
Write Operation	90.369%	89.199%	96.973%

Static noise margin (SNM) is a measure of invulnerability to bit flipping mechanism during read operation. SNM is calculated by seeing the characteristics of cross-coupled inverter during read operation. The bar graph in fig. 15 show the comparison of SNM for 6T CMOS SRAM cell and 6T FinFET SRAM cell at 45nm, 32nm and 16nm.

6. CONCLUSIONS

This paper presents performance analysis of 6T FinFET based SRAM cell at nanoscaled technologies viz. 45nm, 32nm and 16nm. The results have been compared with 6T CMOS SRAM cell in terms of Power Delay Product (PDP) and Static Noise Margin (SNM) performance parameters. Transient analysis of all structures has been carried out for *standby*, *read* and *write* operation of SRAM cell and average power and delay are computed. The simulation results shows reduction in power delay product by 87.5%, 88.8% and 99.1% in read operation and 90.4%, 89.2% and 96.9% in write operation of FinFET based SRAM cell at 45nm, 32nm and 16nm technology nodes respectively as compared to 6T CMOS SRAM cell. The simulation results shown improvement in static noise margin by 27.5%, 31.5% and 8.9% of FinFET based SRAM cell at 45nm, 32nm and 16nm technology nodes respectively as compared to 6T CMOS SRAM cell.

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